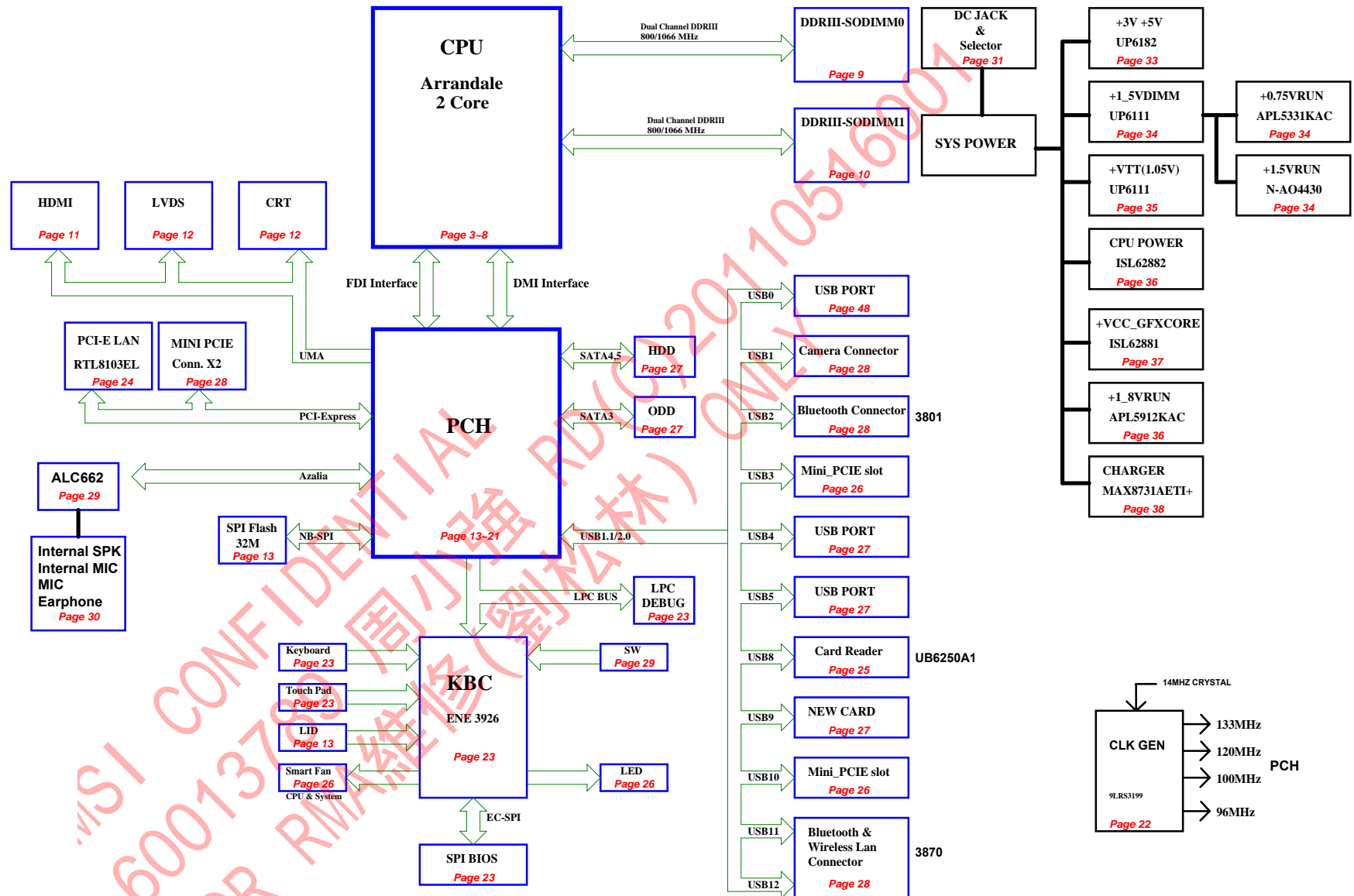


Calpella Platform

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

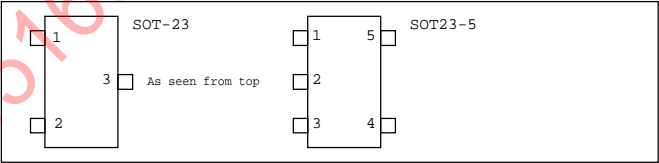
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	LAN
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	DDRIII core
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0	PCH DDRIII command & control pull up. CPU core rail Graphics core rail (Dual Core only)
VTT	1.05V	S0	
+0_75VRUN	0.75V	S0	
+VCC_CORE	1.05V~1.1V	S0	
+VCC_GFXCORE	1.1V	S0	

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



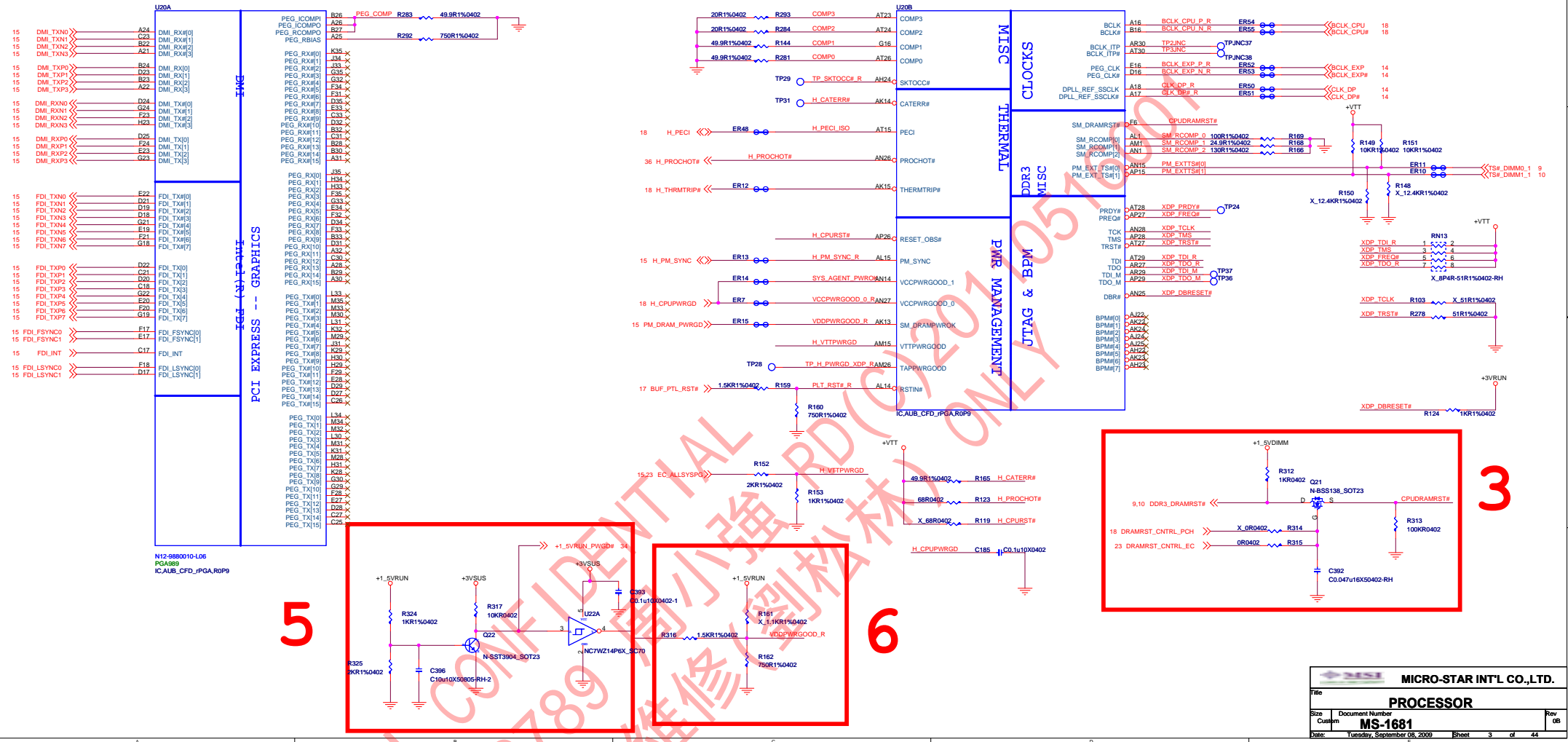
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

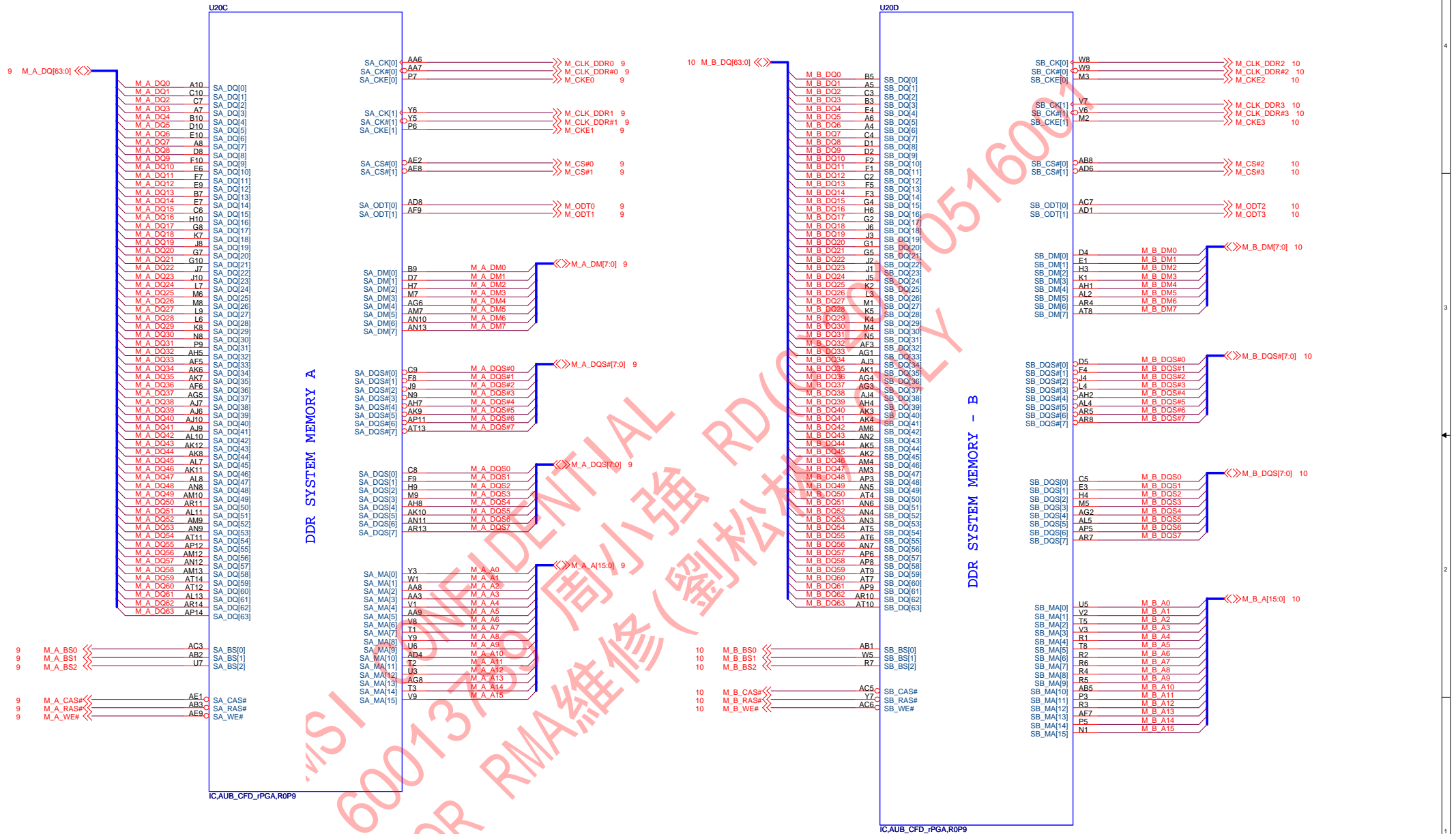
Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

ARRANDALE PROCESSOR (CLK,MISC,JTAG)



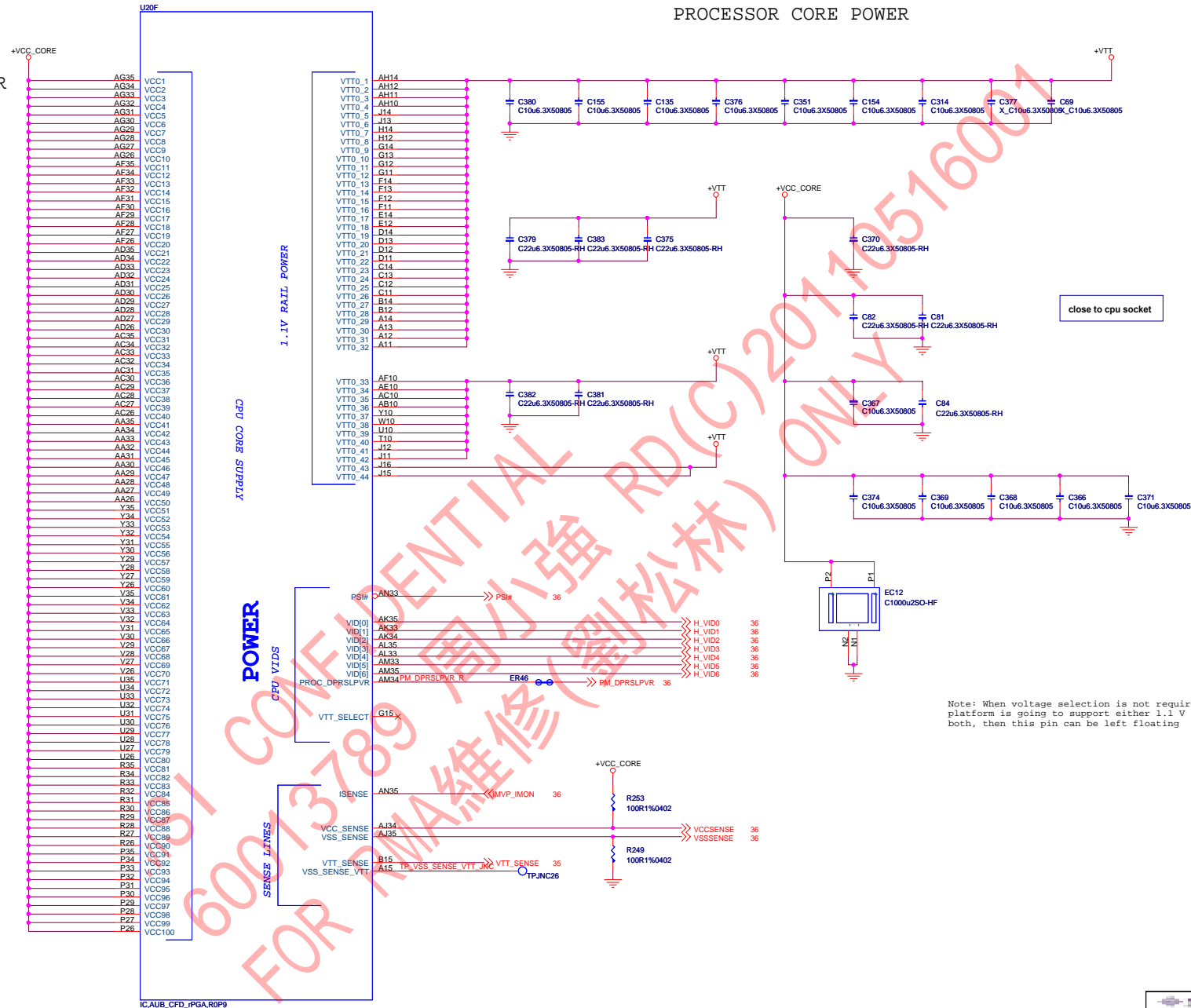
ARRANDALE PROCESSOR (DDR3)



ARRANDALE PROCESSOR (POWER)

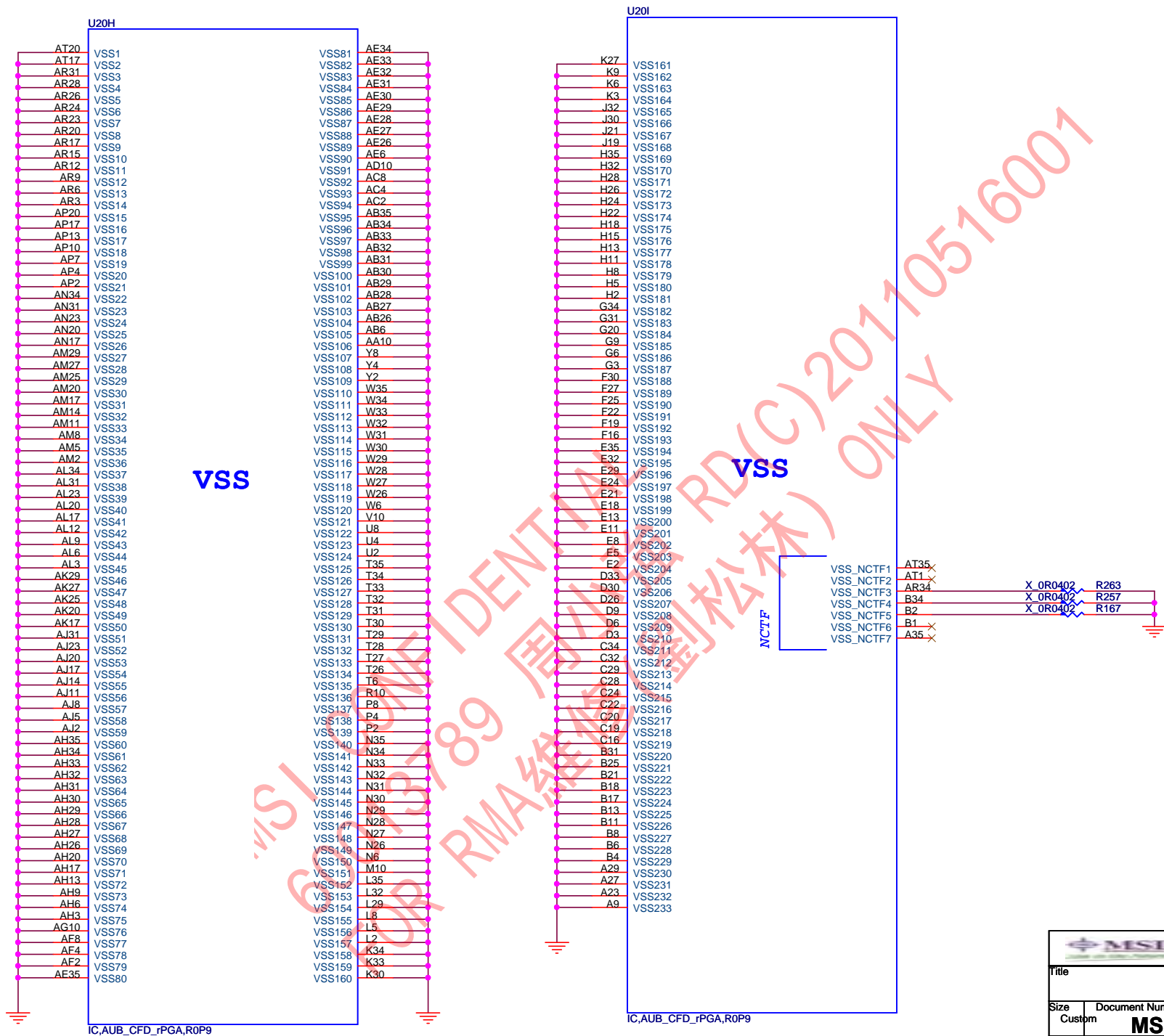
PROCESSOR CORE POWER

PROCESSOR CORE POWER

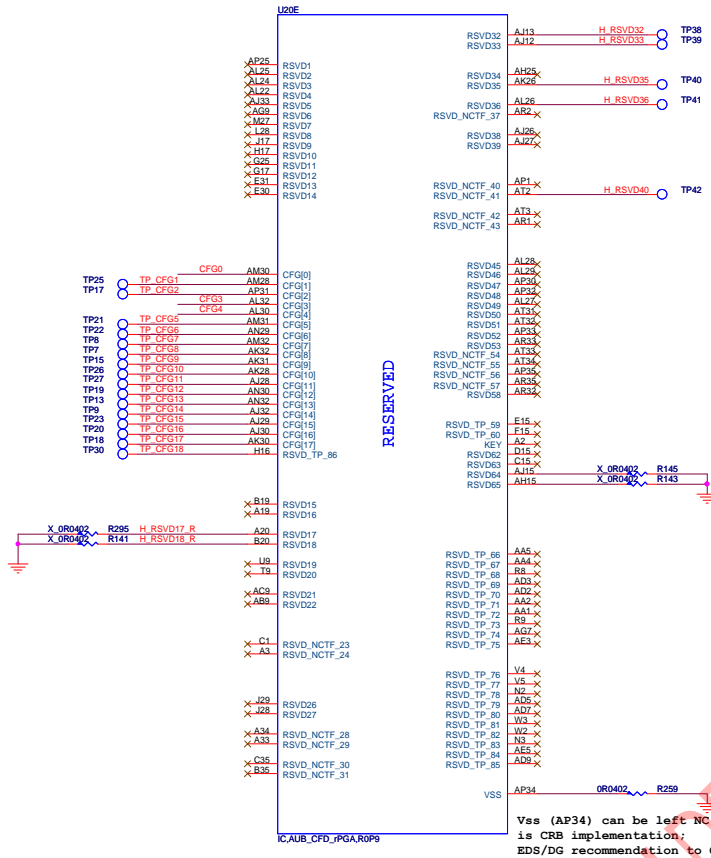


Note: When voltage selection is not required and the platform is going to support either 1.1 V or 1.05 V and not both, then this pin can be left floating

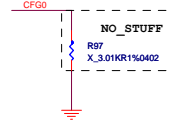
ARRANDALE PROCESSOR (GND)



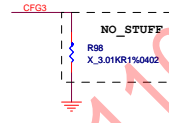
ARRANDALE PROCESSOR (RESERVED)



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Surfation enabled

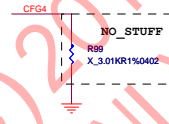


CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversad 15 -> 0, 14 -> 1, ...



CFG[3] - PCI Express* Static Lane
Numbering Reversal. Lane Reversal will be
applied across all 16 Lanes.
1: No lane reversal
0: Reversal

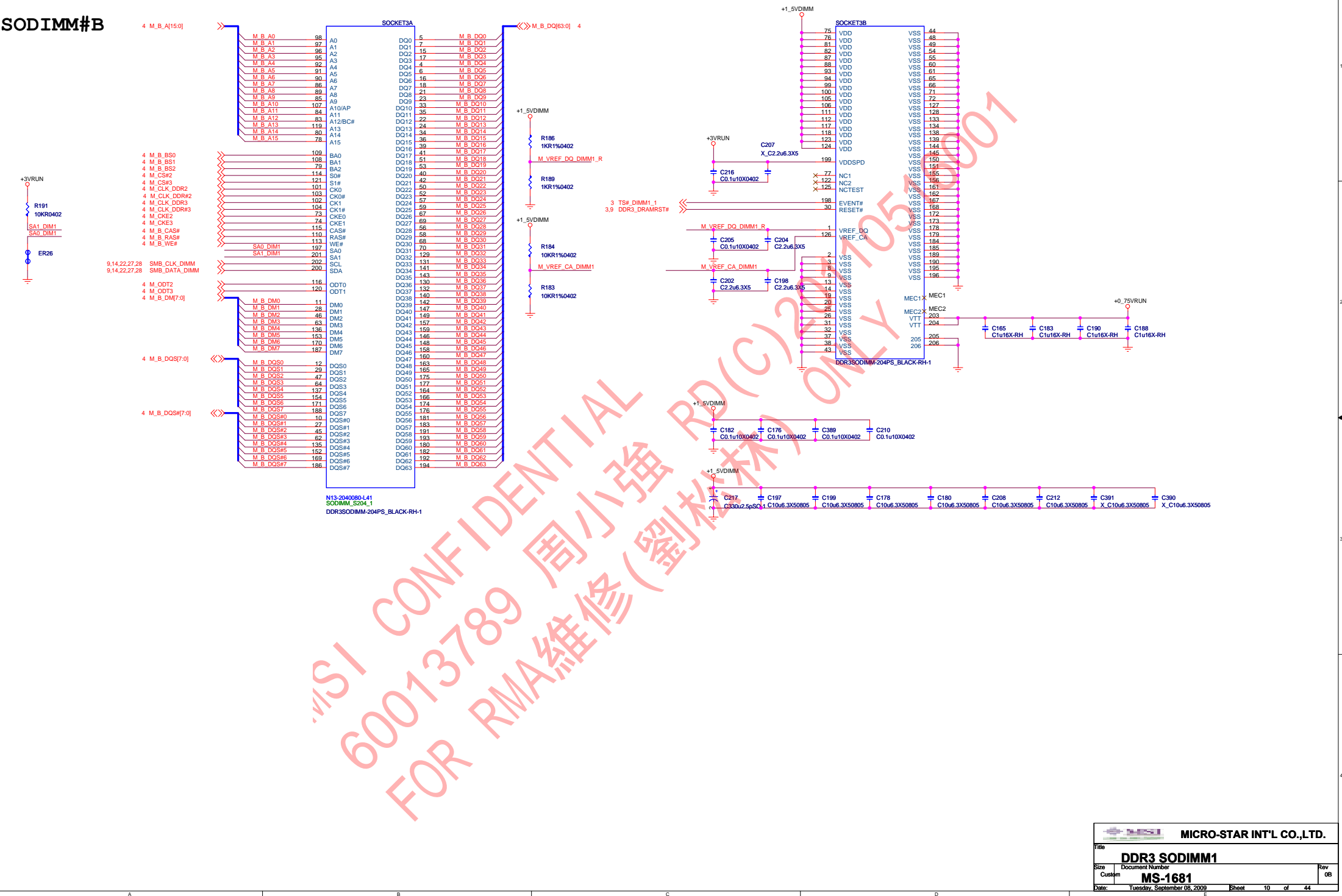
CFG4 - Display Port Presence	
CFG4	1:Disabled: No Physical Display Port attached to Embedded Display Port 0:Enabled: An external Display Port device is connected to the Embedded Display Port



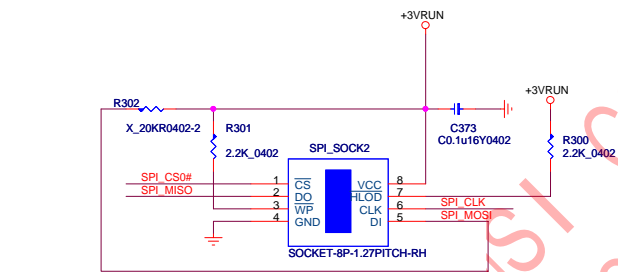
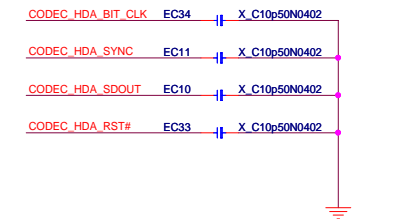
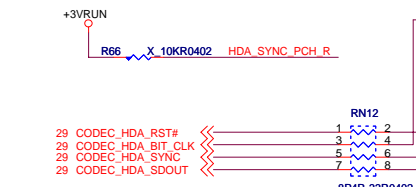
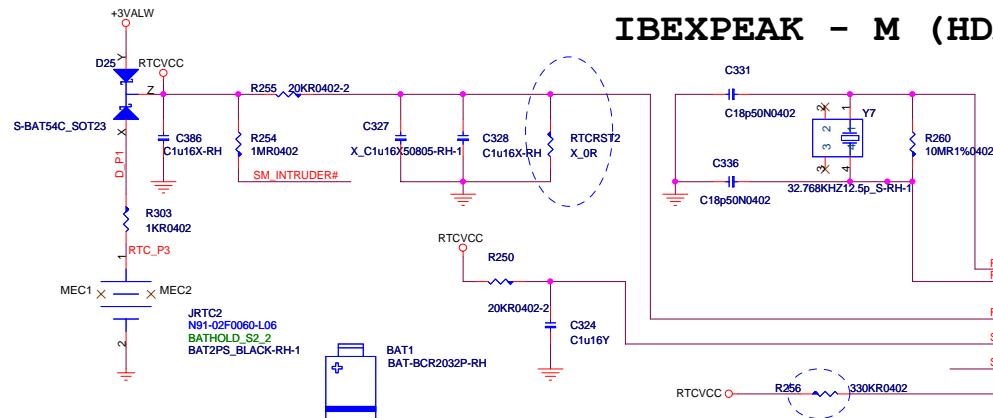
Layout Note:
Location of all CFG strap resistors needs
to be close to trace to minimize stub

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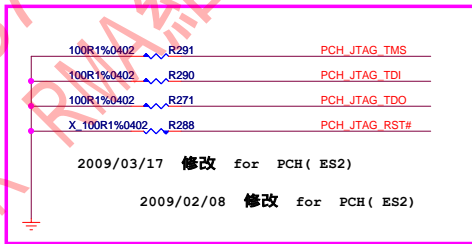
SODIMM#B



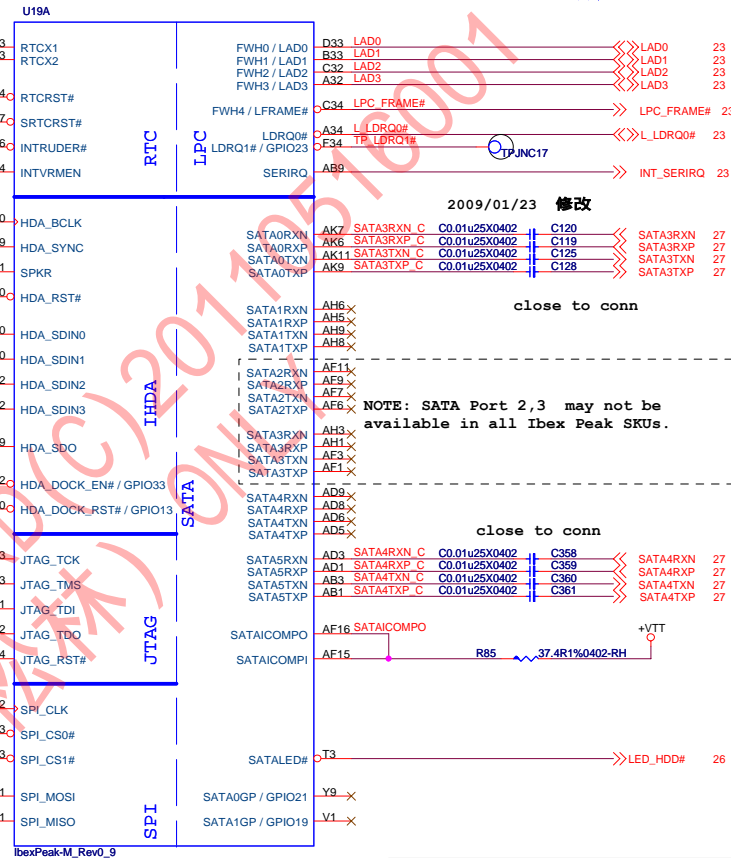
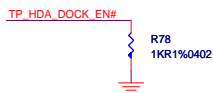
IBEXPEAK - M (HDA, JTAG, SATA)



SPI_MOSI :Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor
Disable iTPM: Left floating, no pull-down required.



2009/03/17 修改 for PCH(ES2)
2009/02/08 修改 for PCH(ES2)



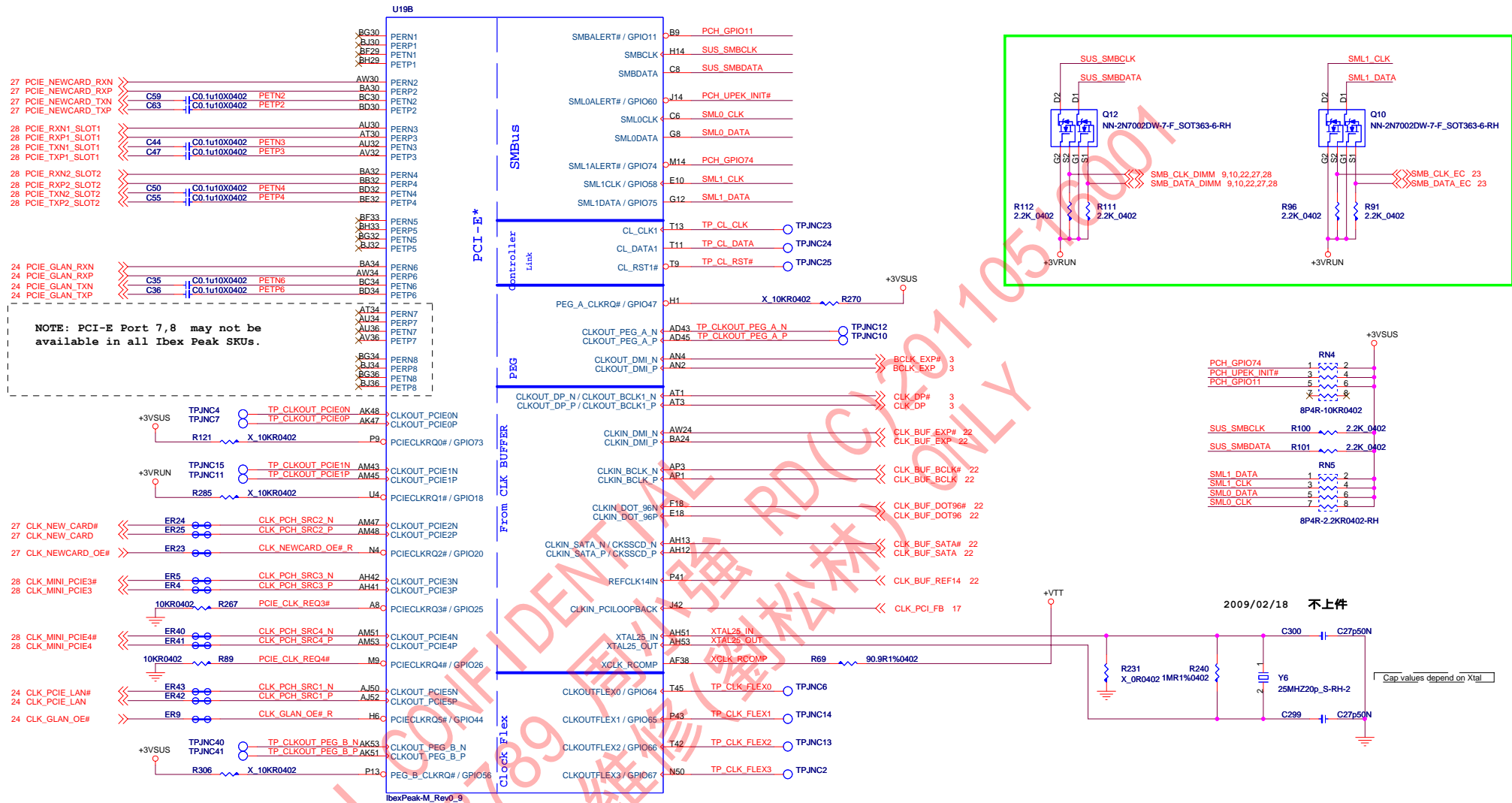
2009/01/23 修改
close to conn

NOTE: SATA Port 2,3 may not be available in all Ibex Peak SKUs.

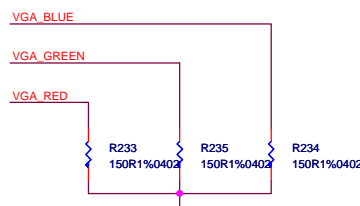
close to conn
HDD

PCH PIN	REFDES	ES2	STATE
TDO	R289	200 ohm	STUFF
	R271	100 ohm	STUFF
TMS	R298	200 ohm	STUFF
	R291	100 ohm	STUFF
TDI	R297	200 ohm	STUFF
	R290	100 ohm	STUFF
TCK	R273	51 ohm	STUFF
TRST#	R296	not applicable	NO STUFF
	R288	not applicable	NO STUFF

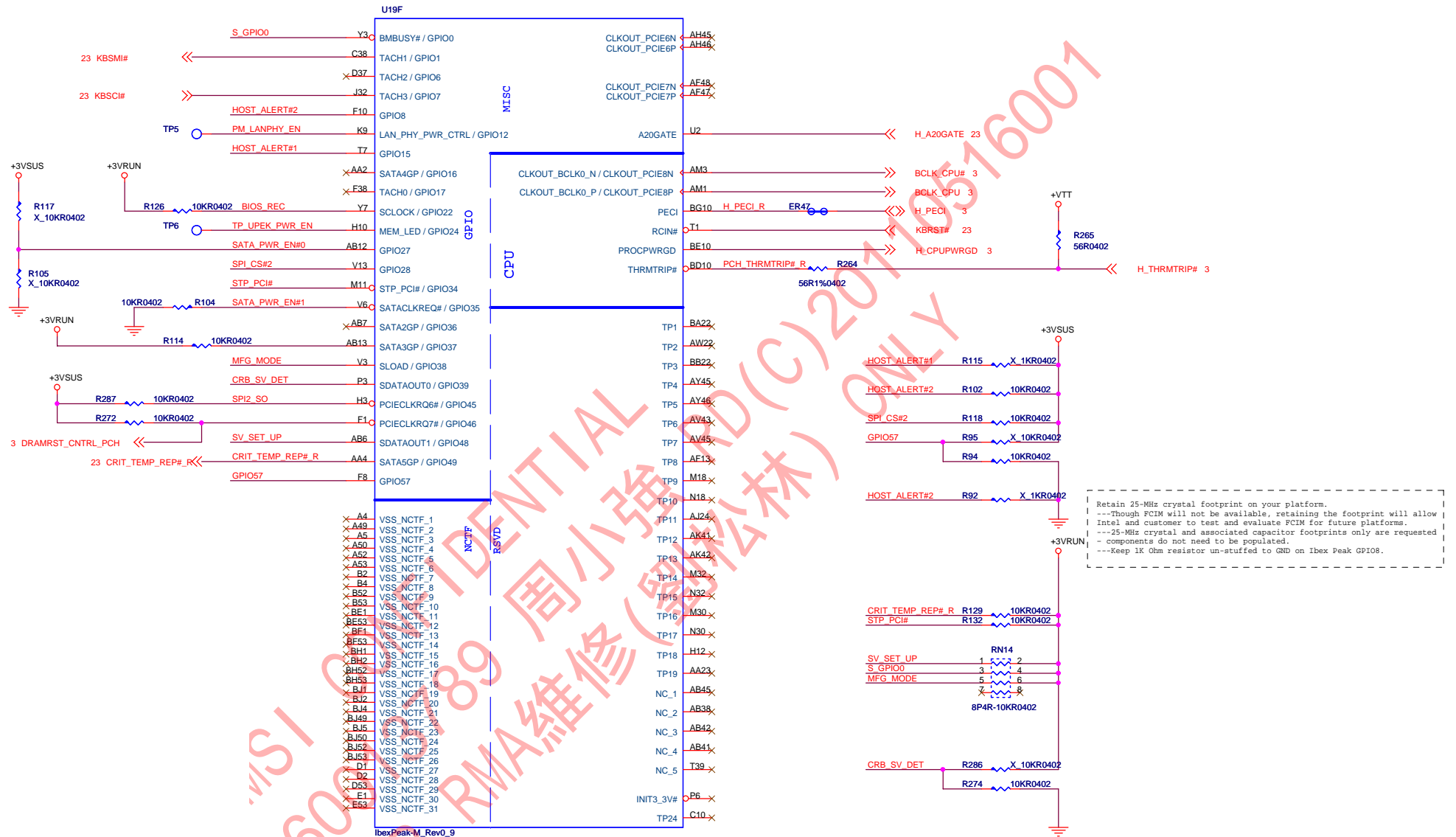
IBEXPEAK - M (PCI-E, SMBUS, CLK)



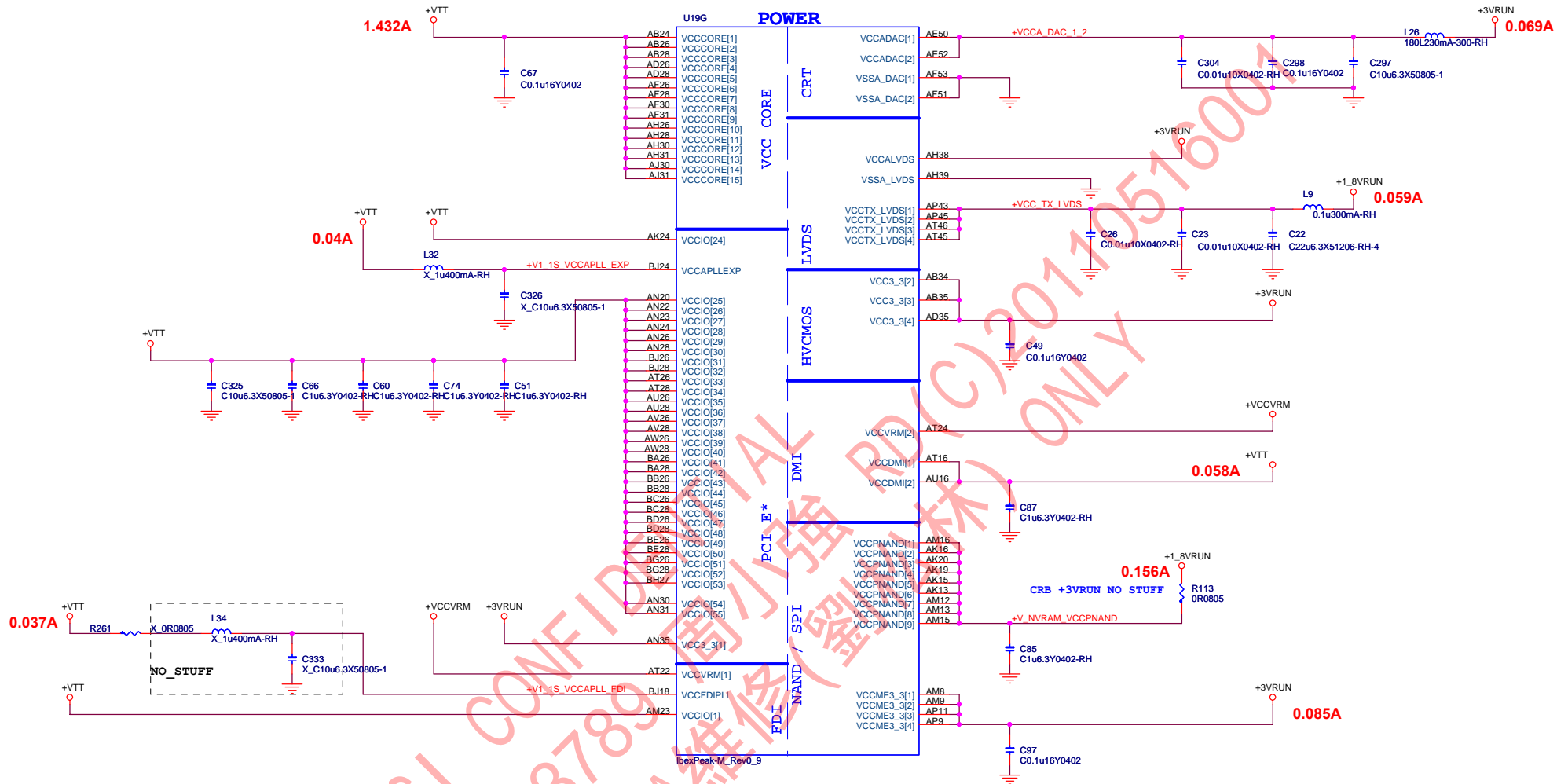
PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well



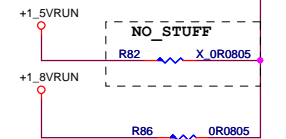
IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)



IBEXPEAK - M (POWER)

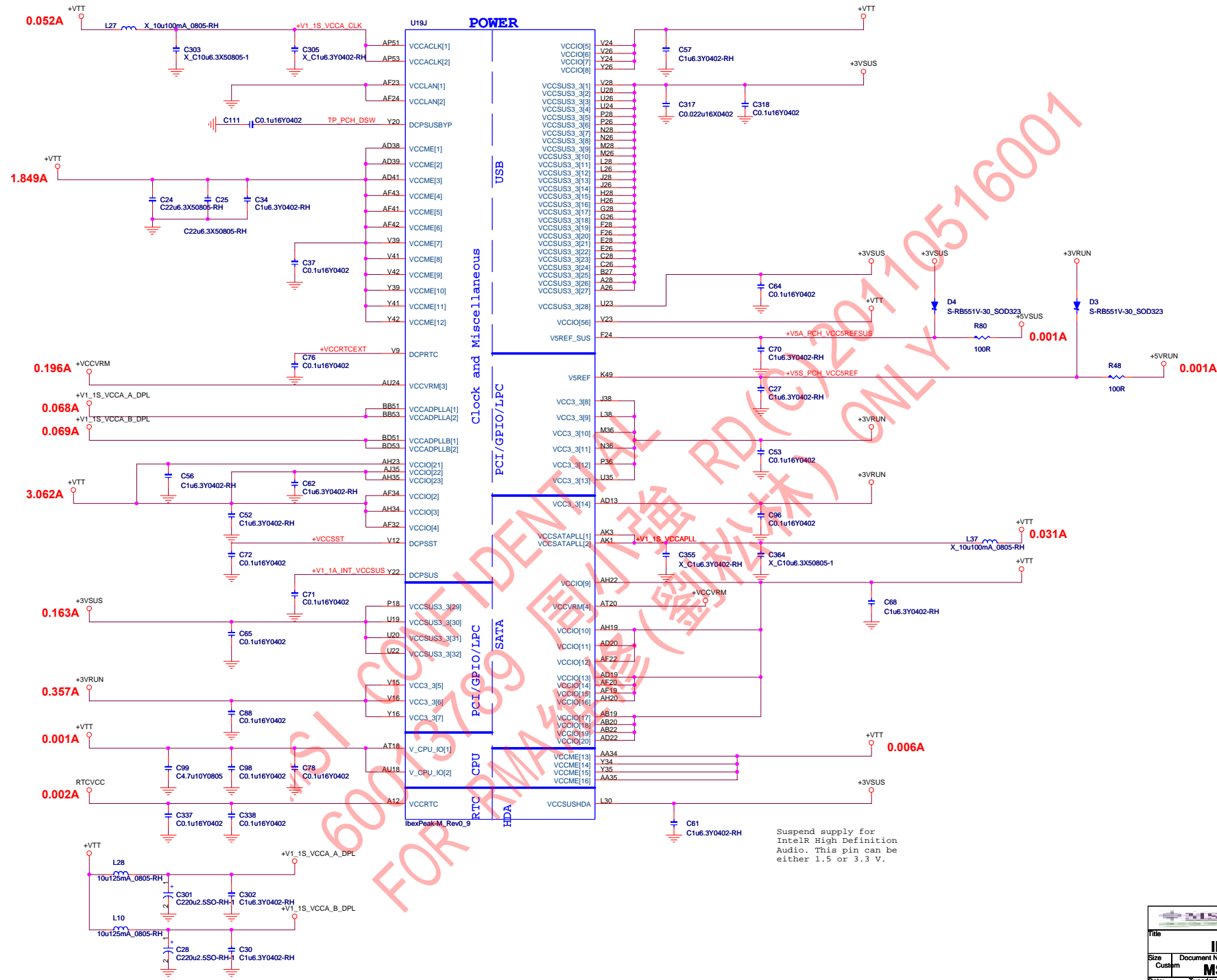


The VCCVPM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVPM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

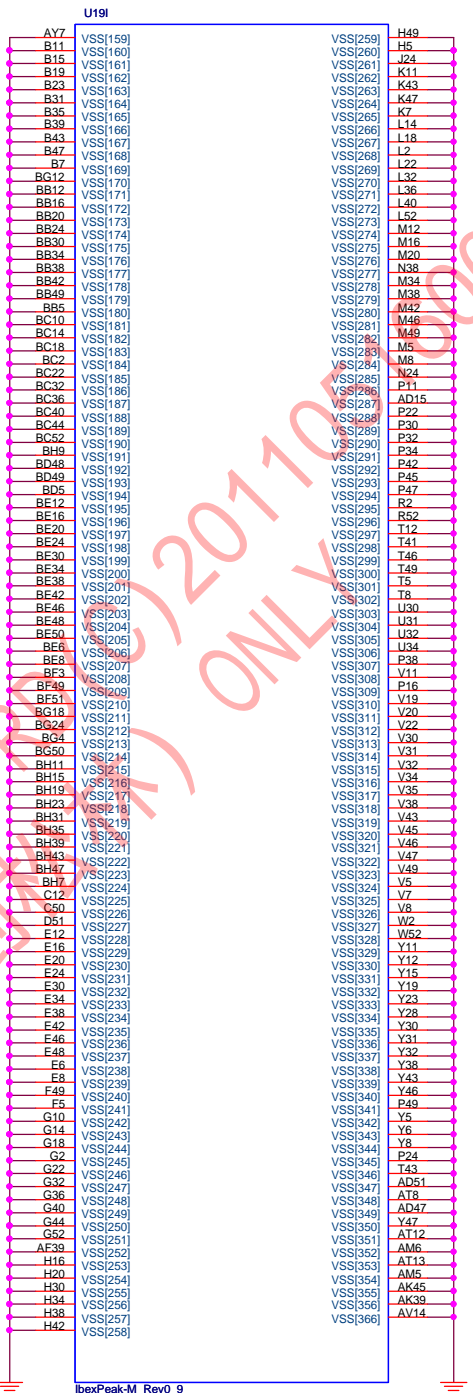
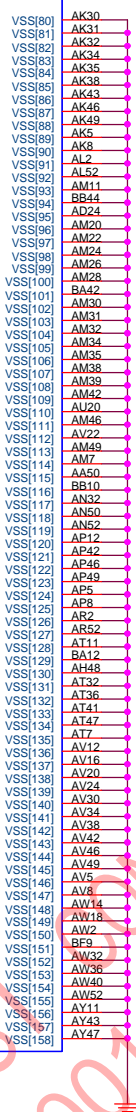
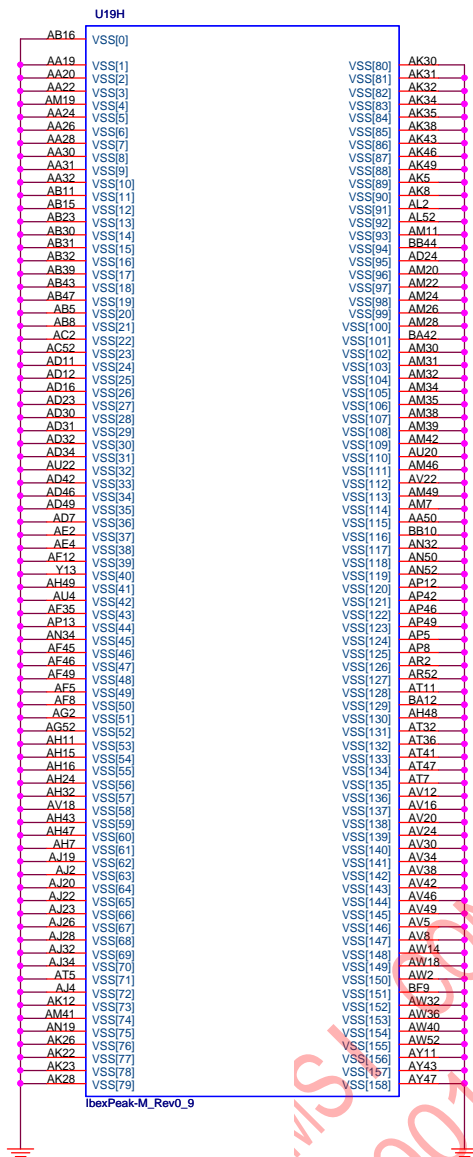


VccLAN may be grounded if Intel LAN is disabled.


IBEXPEAK - M (POWER)



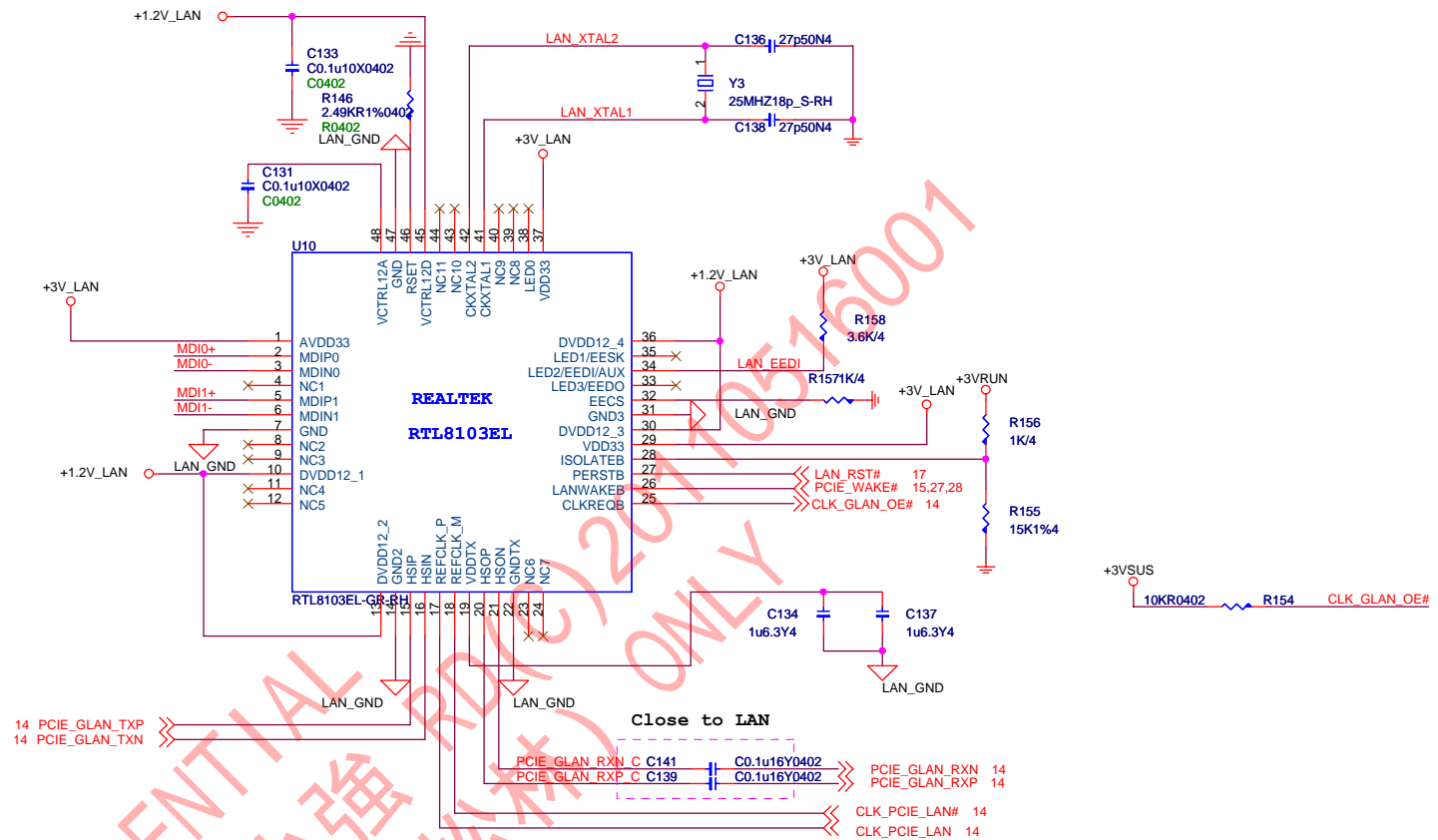
IBEXPEAK - M (GND)



ibexPeak-M_Rev0_9

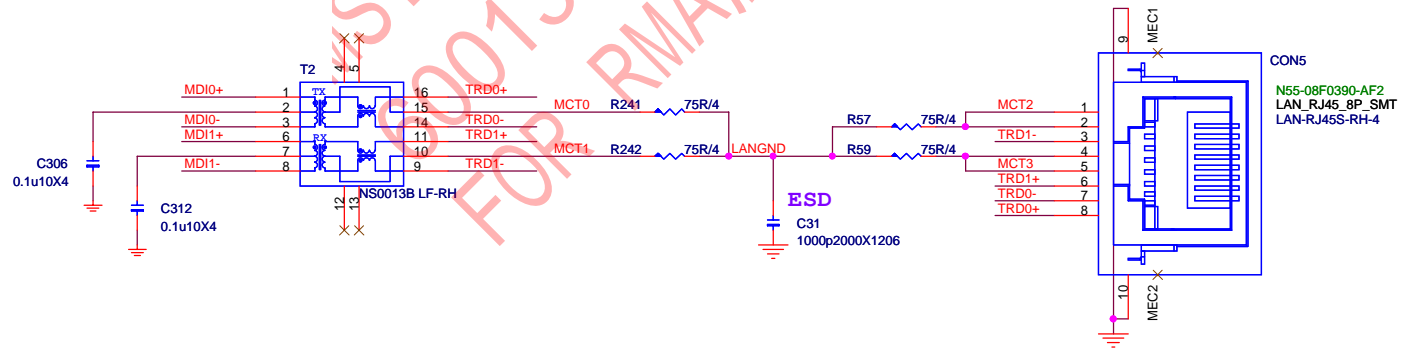
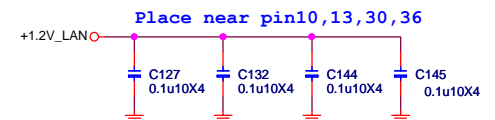
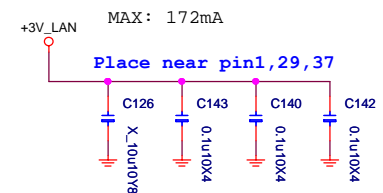
 MICRO-STAR INT'L CO.,LTD.		
IBEXPEAK - M (GND)		
Title Size Custom	Document Number MS-1681	Rev 0B
Date: Tuesday, September 08, 2009 Sheet 21 of 44		

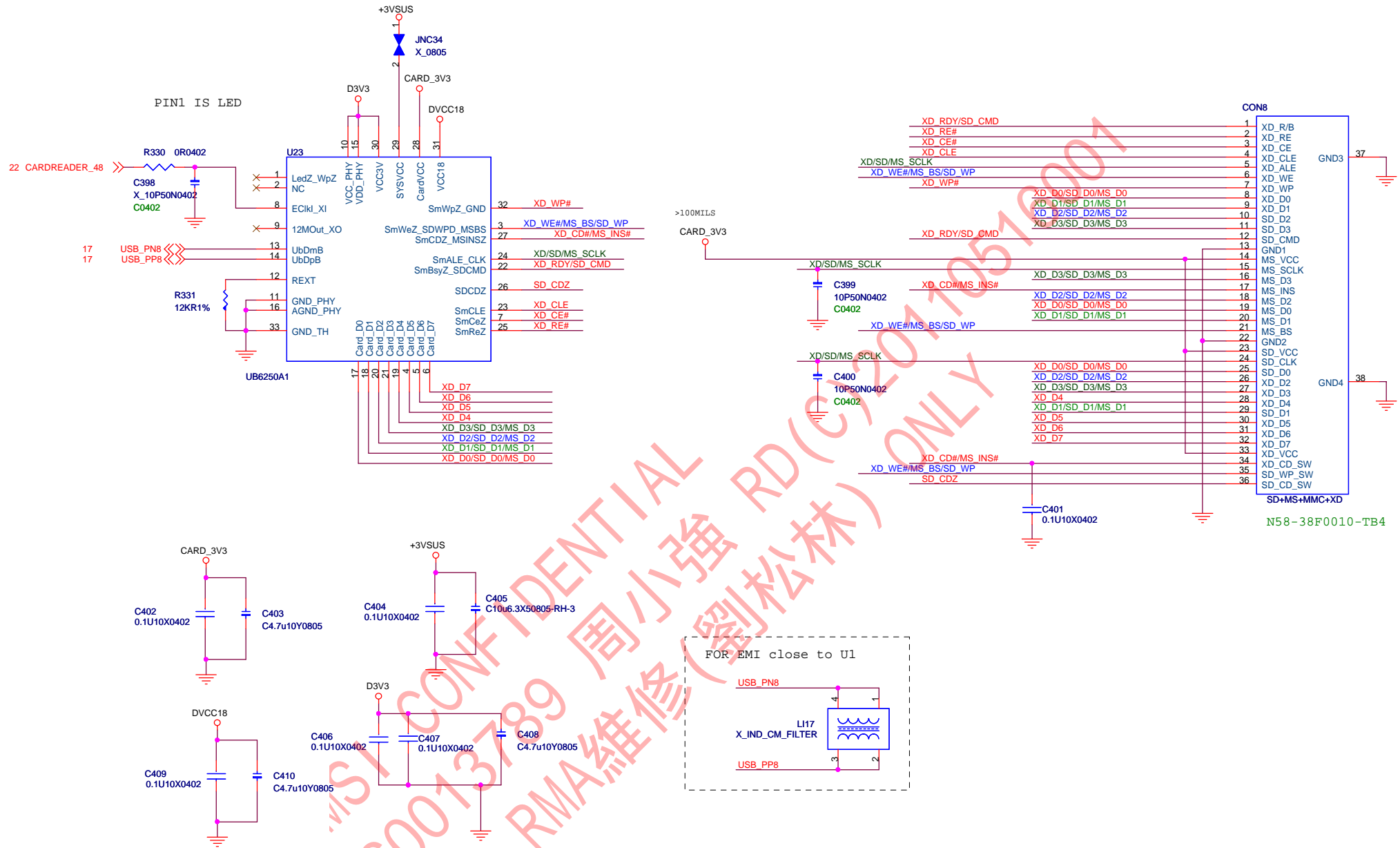
1. Pin 46 : RSET res should be close to LAN chip. Don't have power trace or high frequency trace beside it.
2. The trace of each Pair(MDIX+/-) should be equal in length and better have ground under.
3. Both EGND and GND can be connect together or use 0 Ohm res. to connect them.
4. 1.2V請留 power plane並且盡量大一點.
5. 1.2V Bypass 電容不能省. 在 LAN 的每一個 power pin 都加 0.1u 的電容, 不能省.
6. 請參考RTL8111C EMI layout notice. Fine tune cap (0.1uF ~ 10pF) of center-tapped can improve EMI for single tone noise.
7. Please refer and follow our Layout Guidel.5 as attached file
8. RJ45 的部份, 對應 pin 請您在confirm一下.....一般都是接到 RJ45 pin 12/ 36

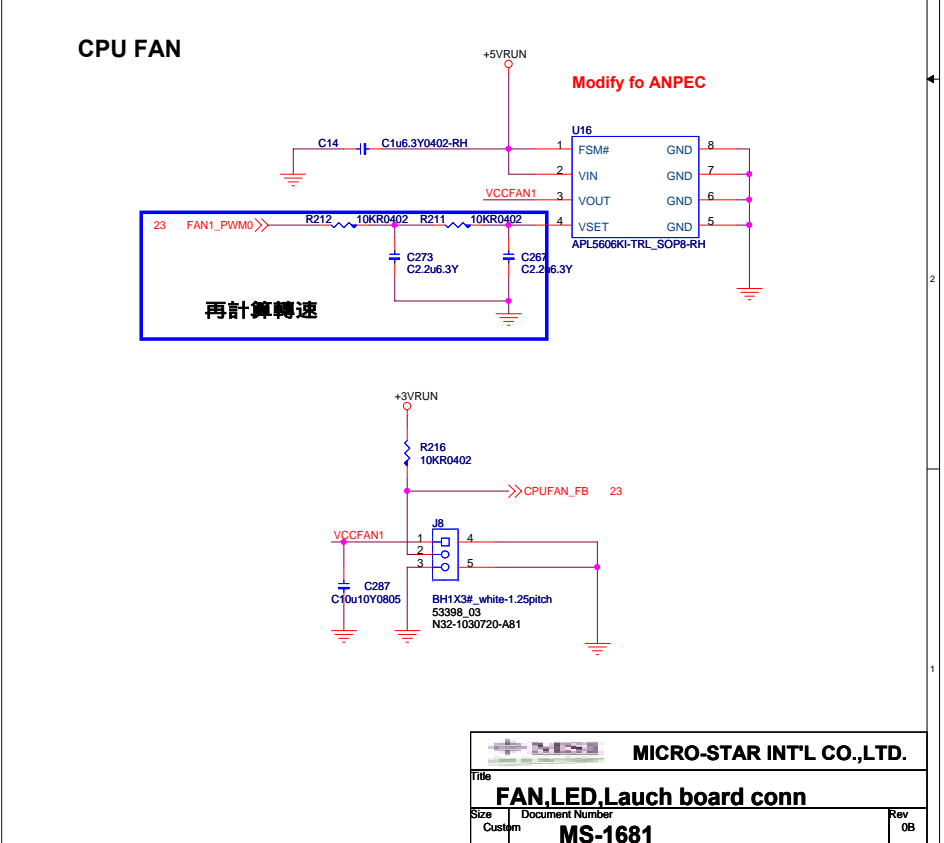
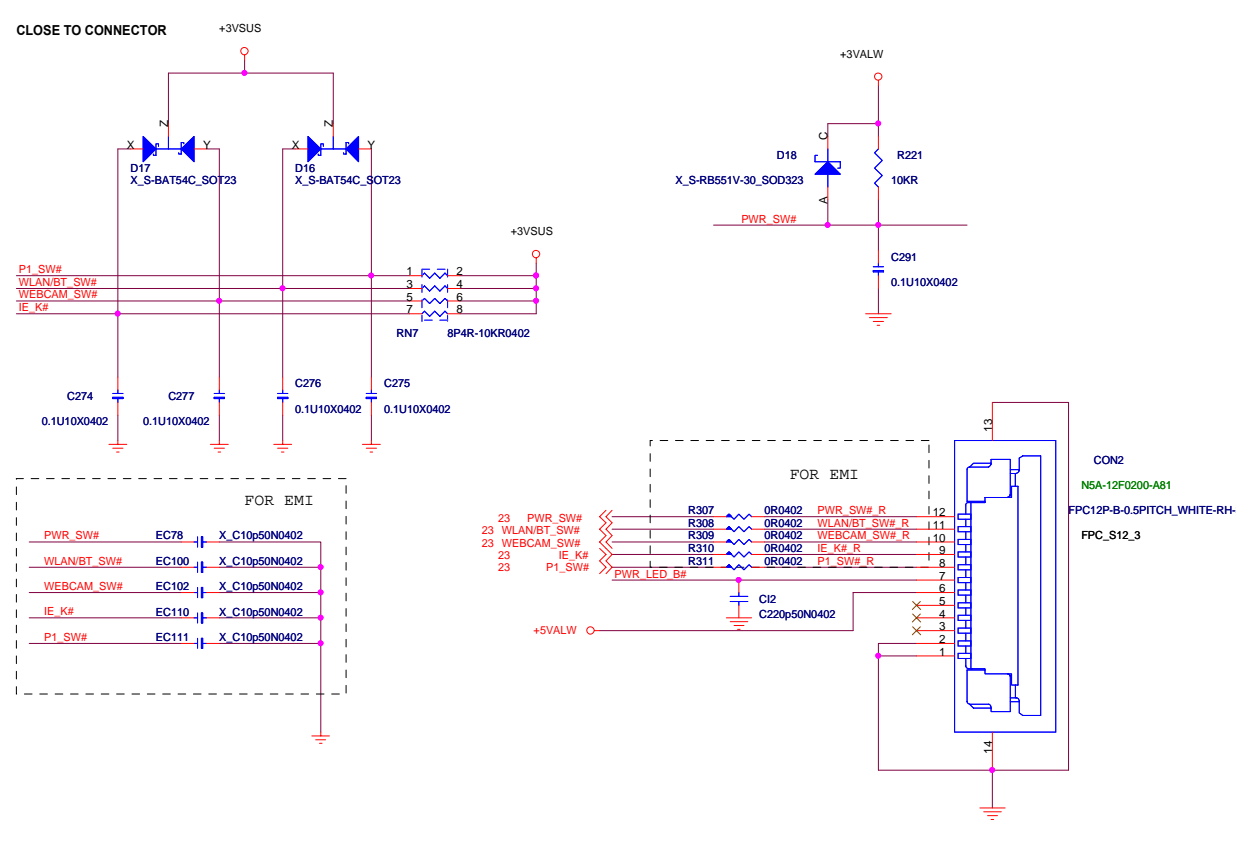
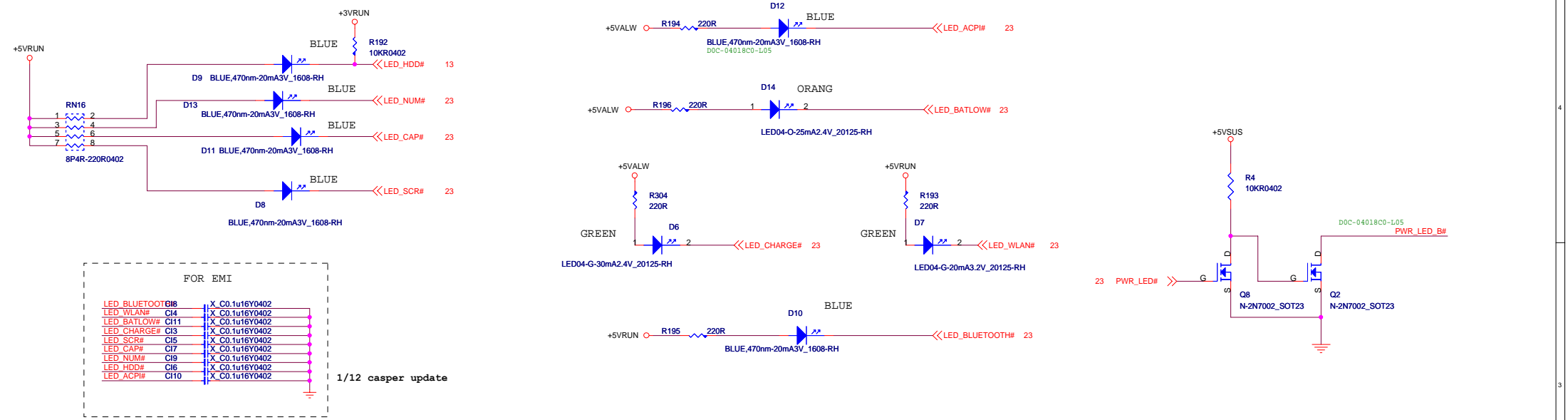


POWER Comparison

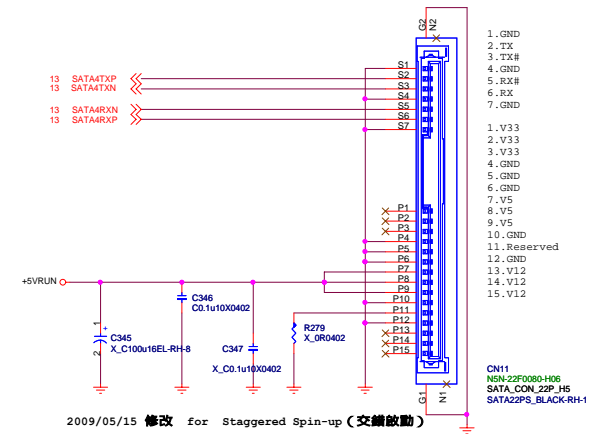
	3.3V	mW
10 M Idle/TxRx	87/172	287/568
100 M Idle/TxRx	112/165	370/545
ALDPS	60	198
D3 cold with link10M /without link	32/18	106/59.4



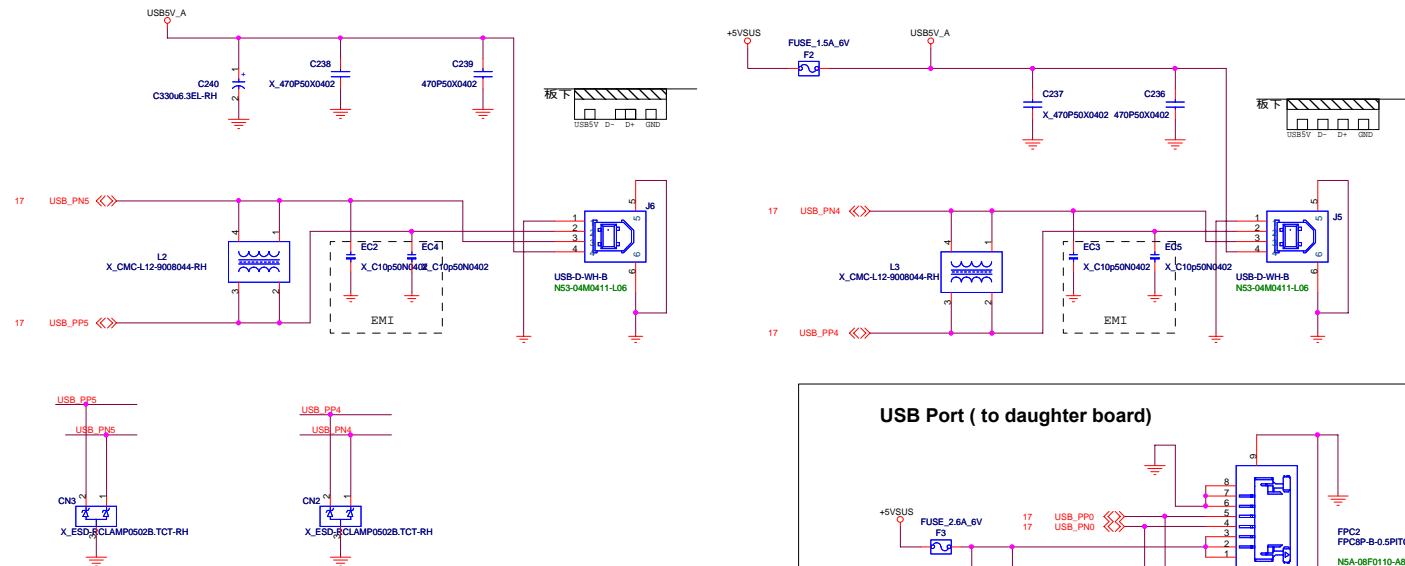




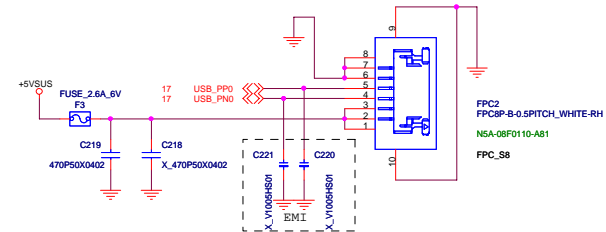
SATA HDD



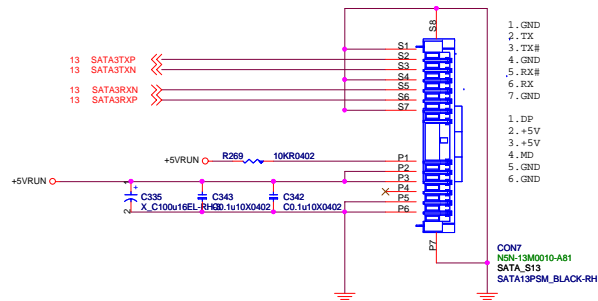
USB Port



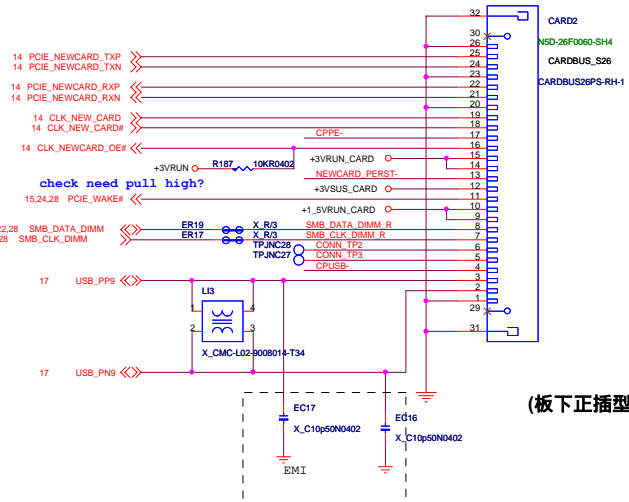
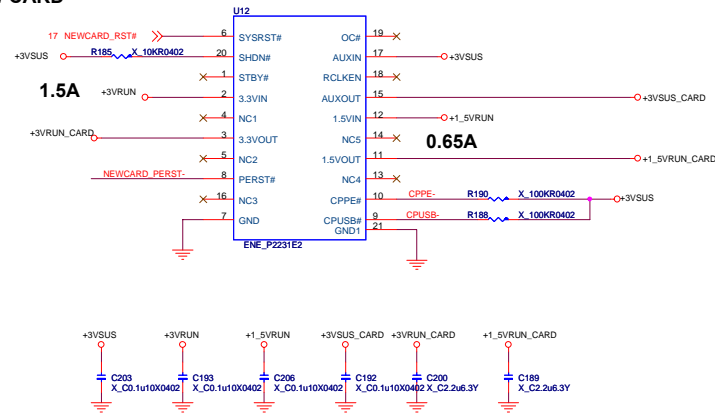
USB Port (to daughter board)



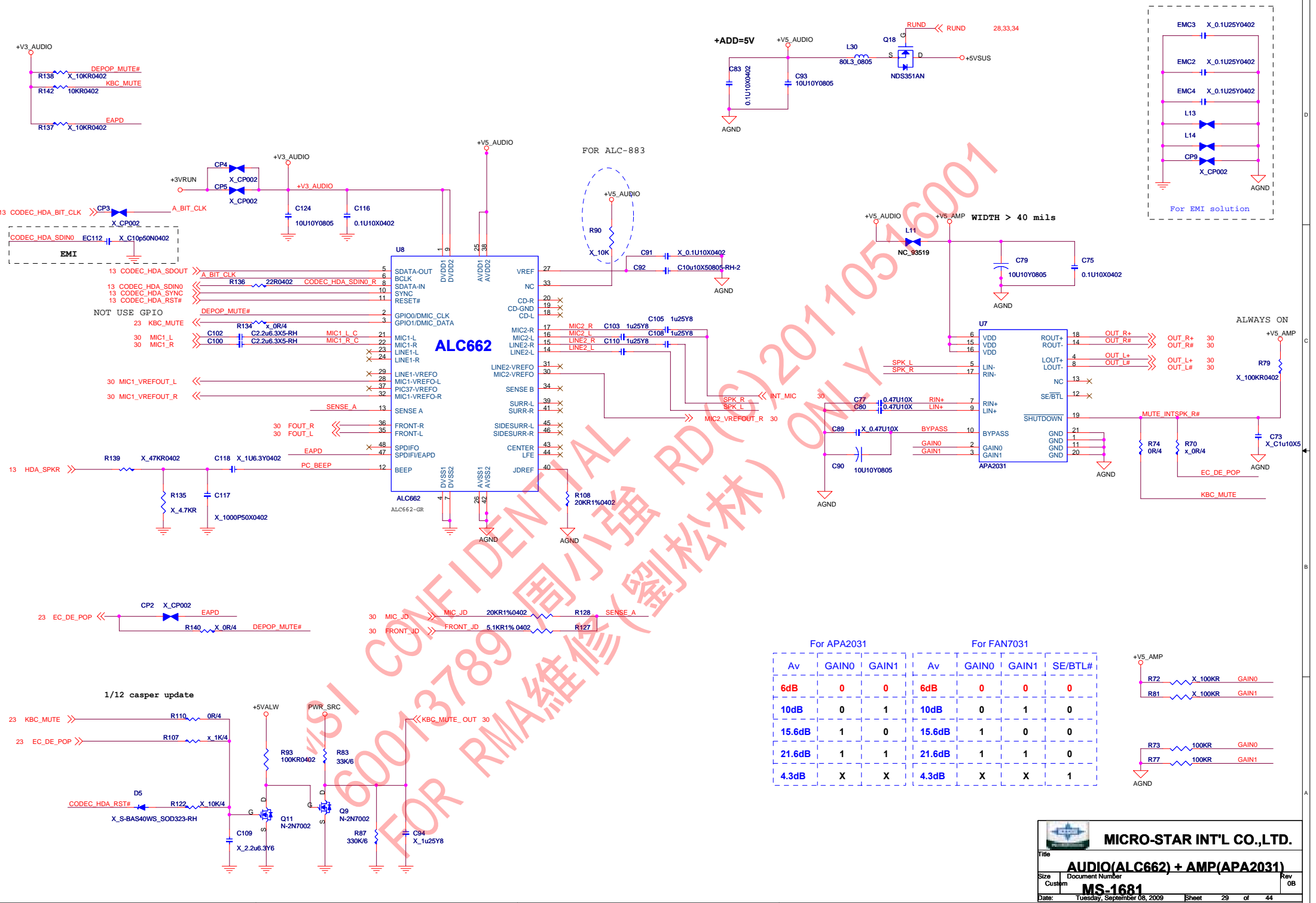
SATA ODD

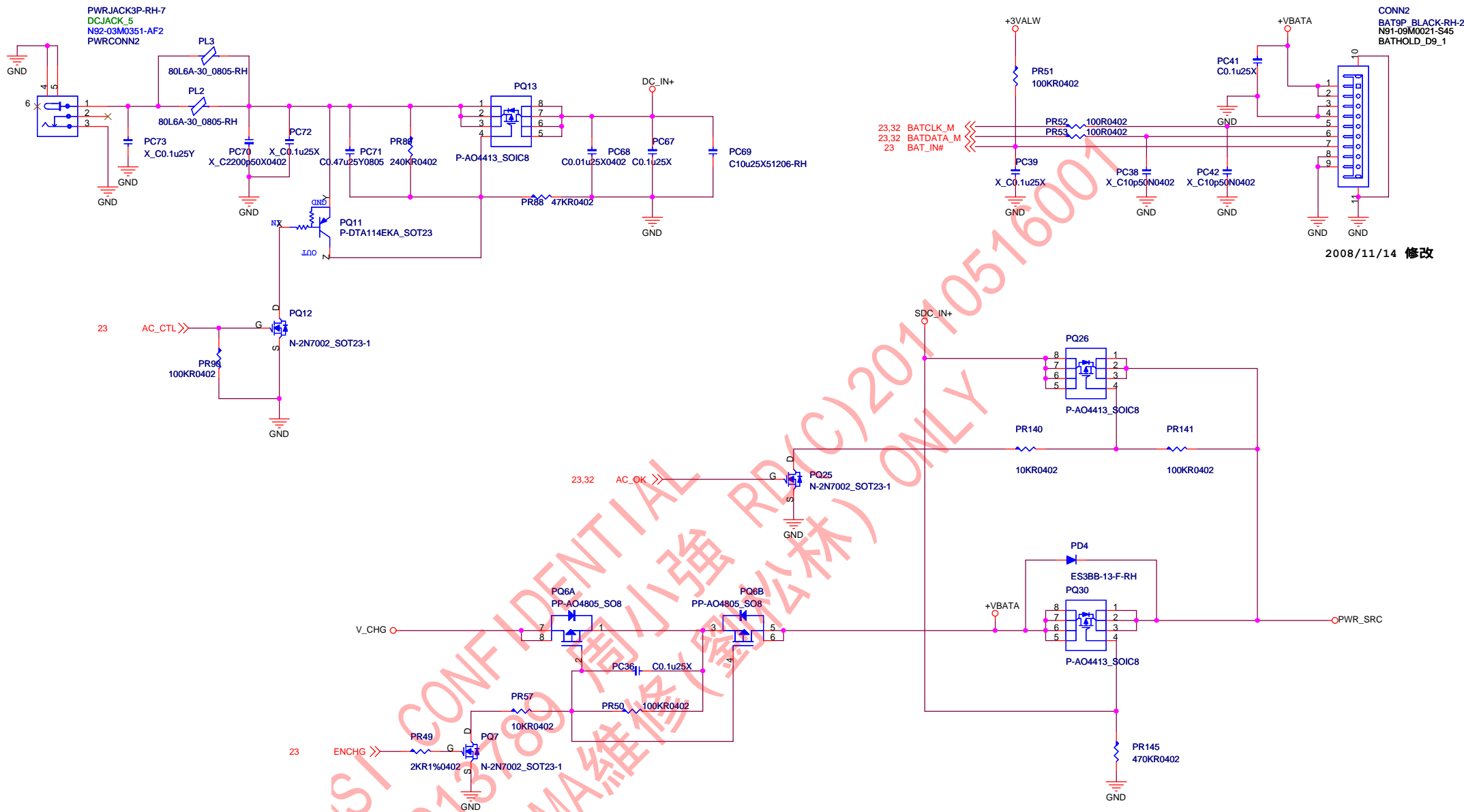


NEW CARD



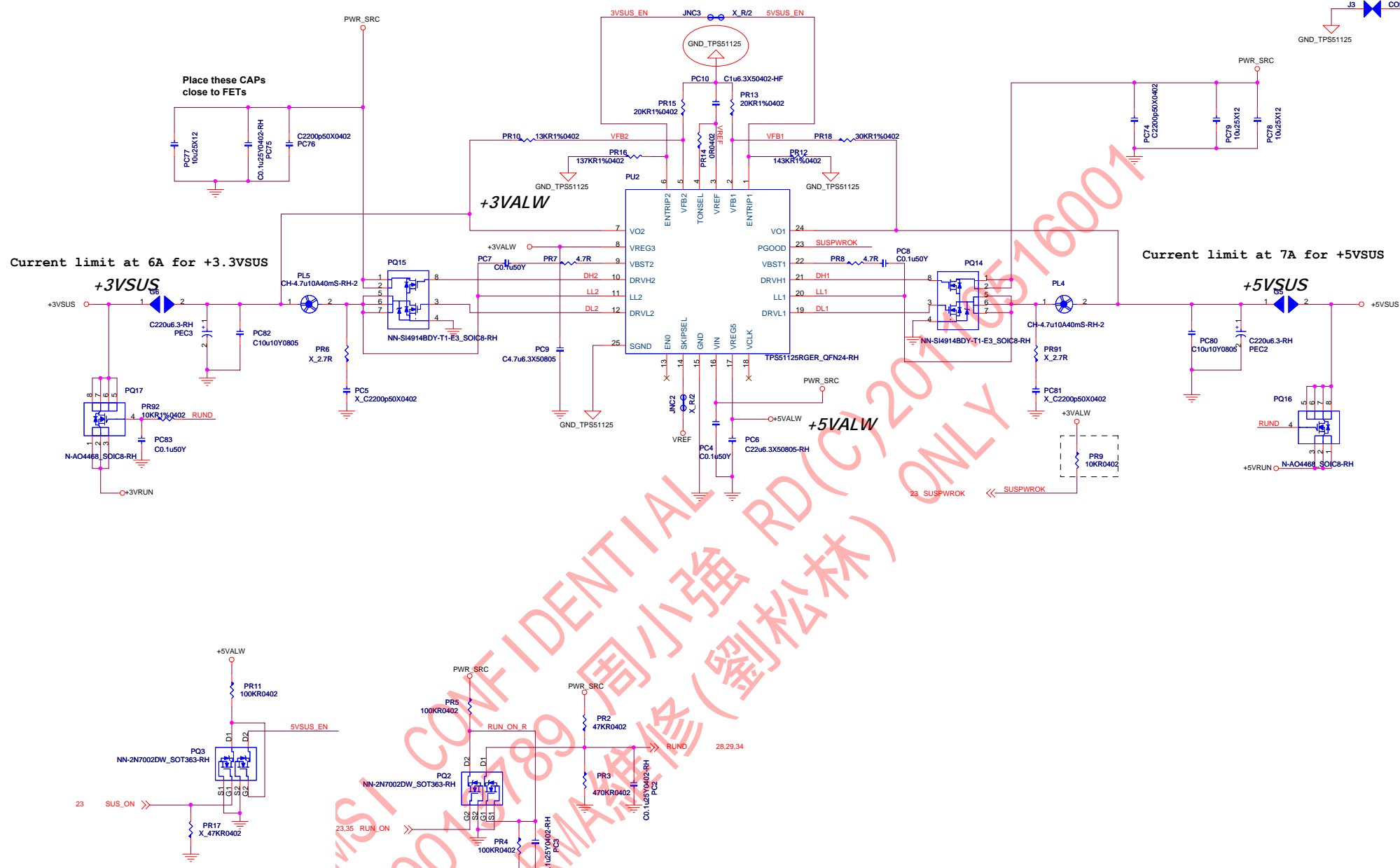
(板下正插型)

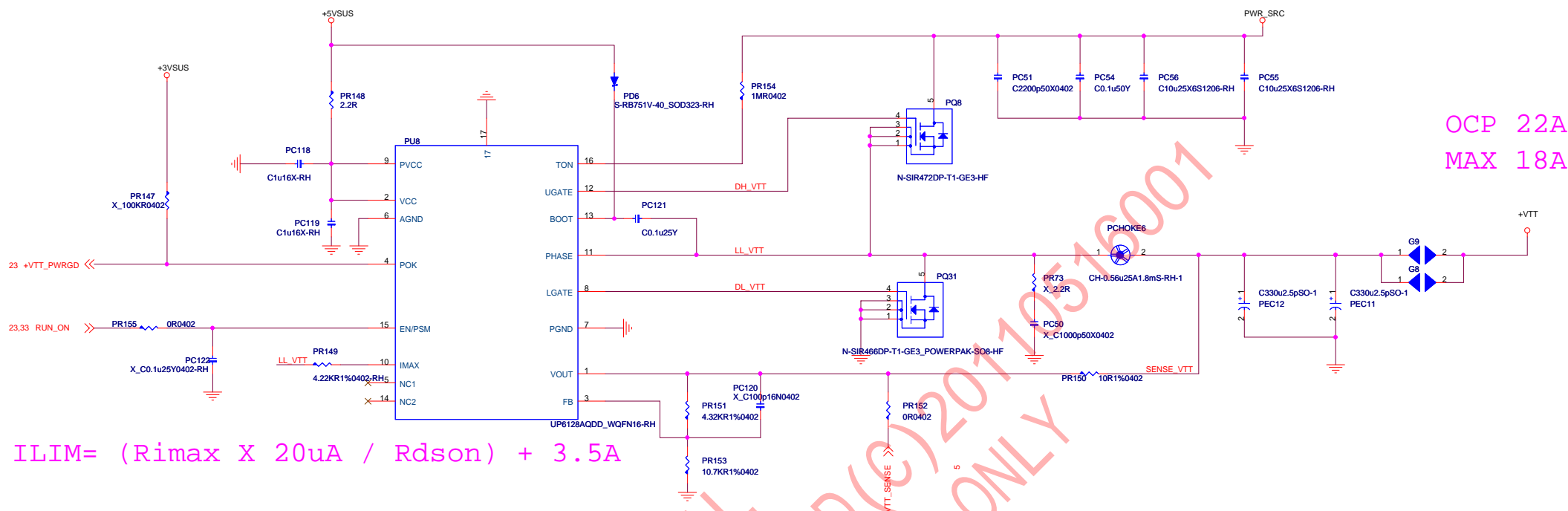




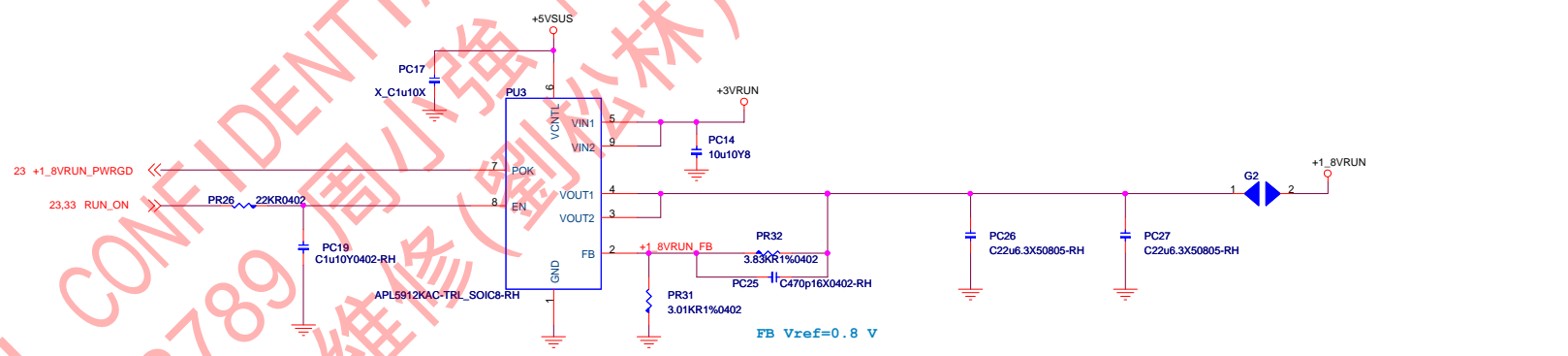
2008/11/14 修改

MSI MICRO-STAR INT'L CO.,LTD.		
Title		
Battery Select		
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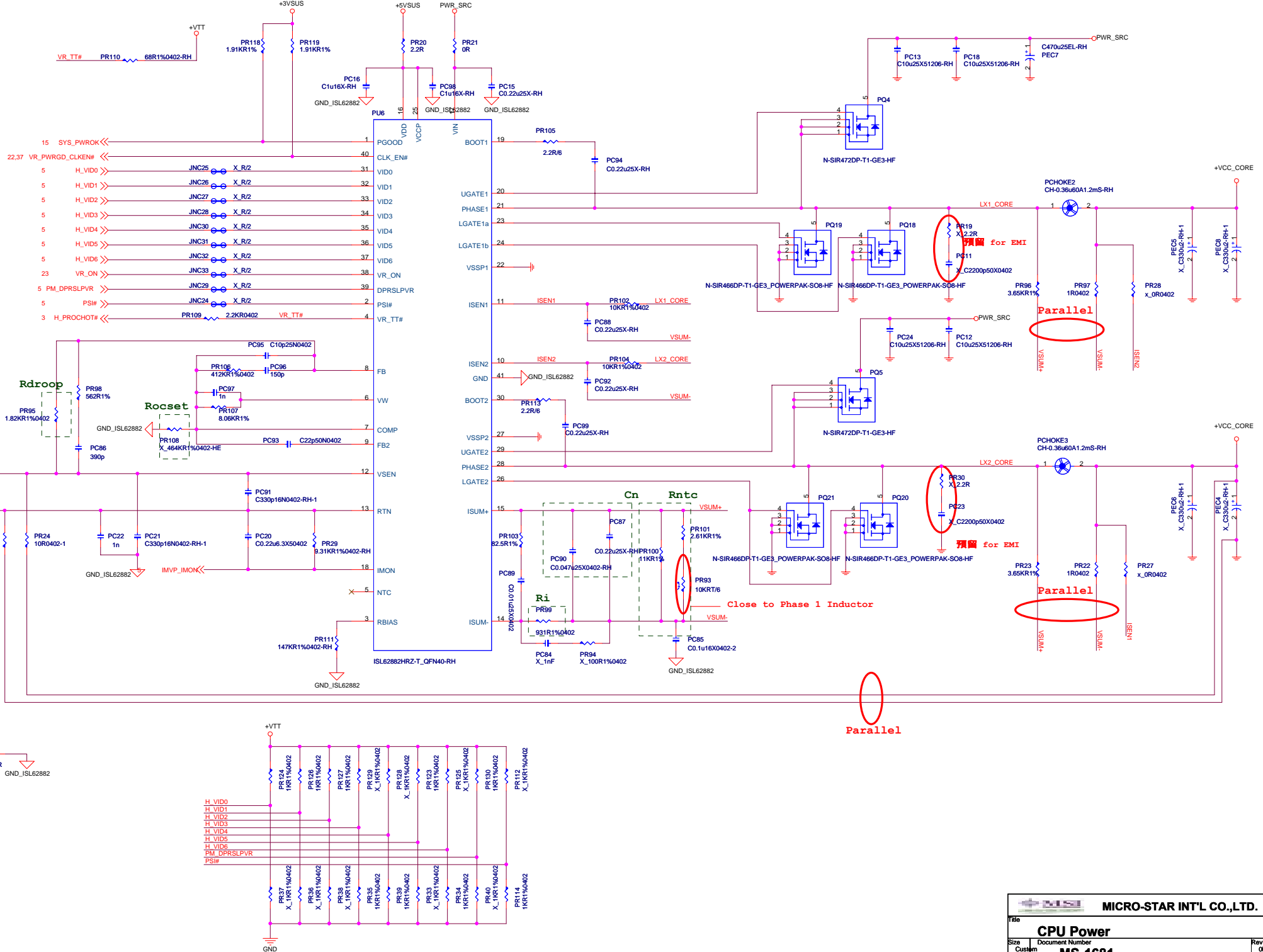


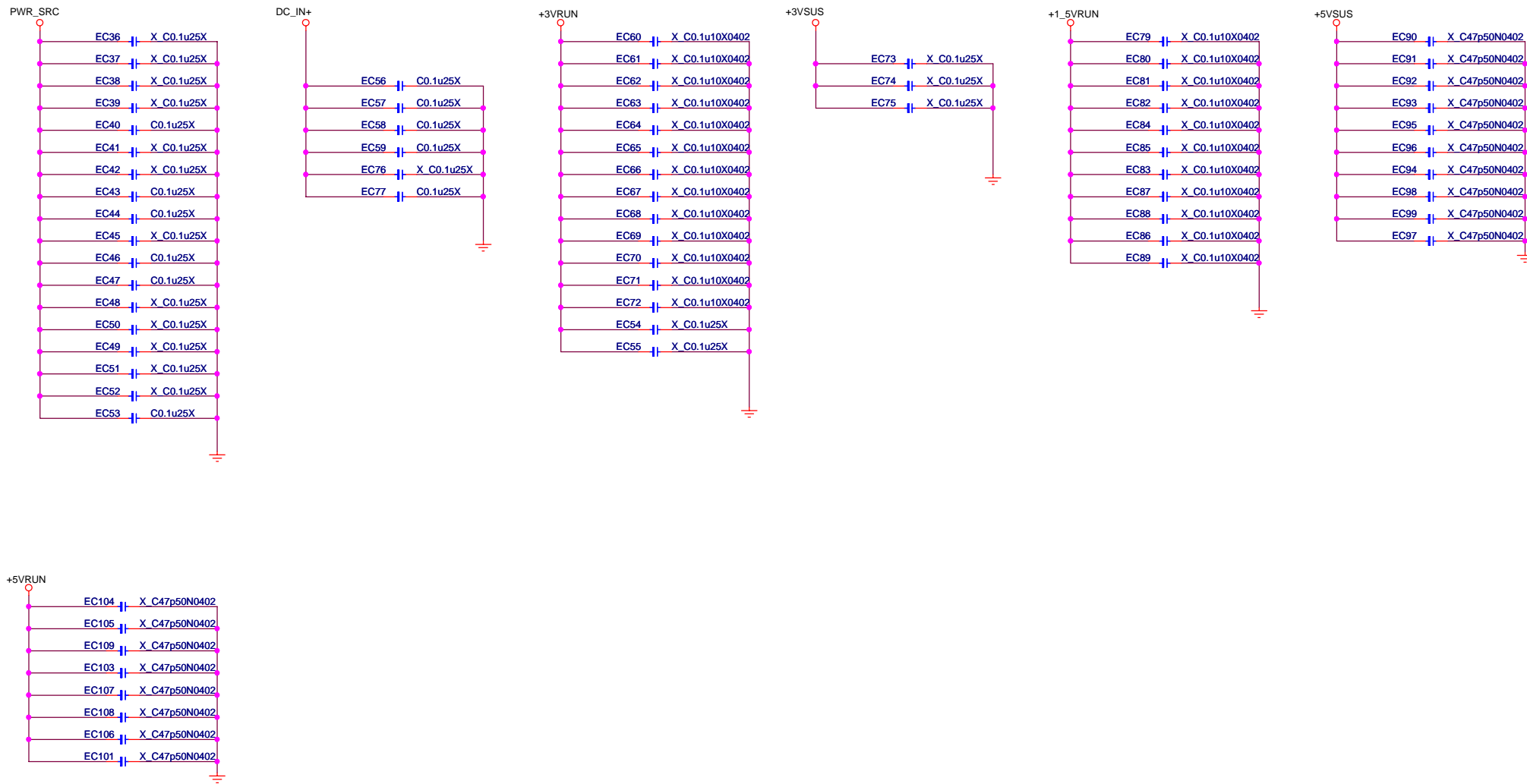


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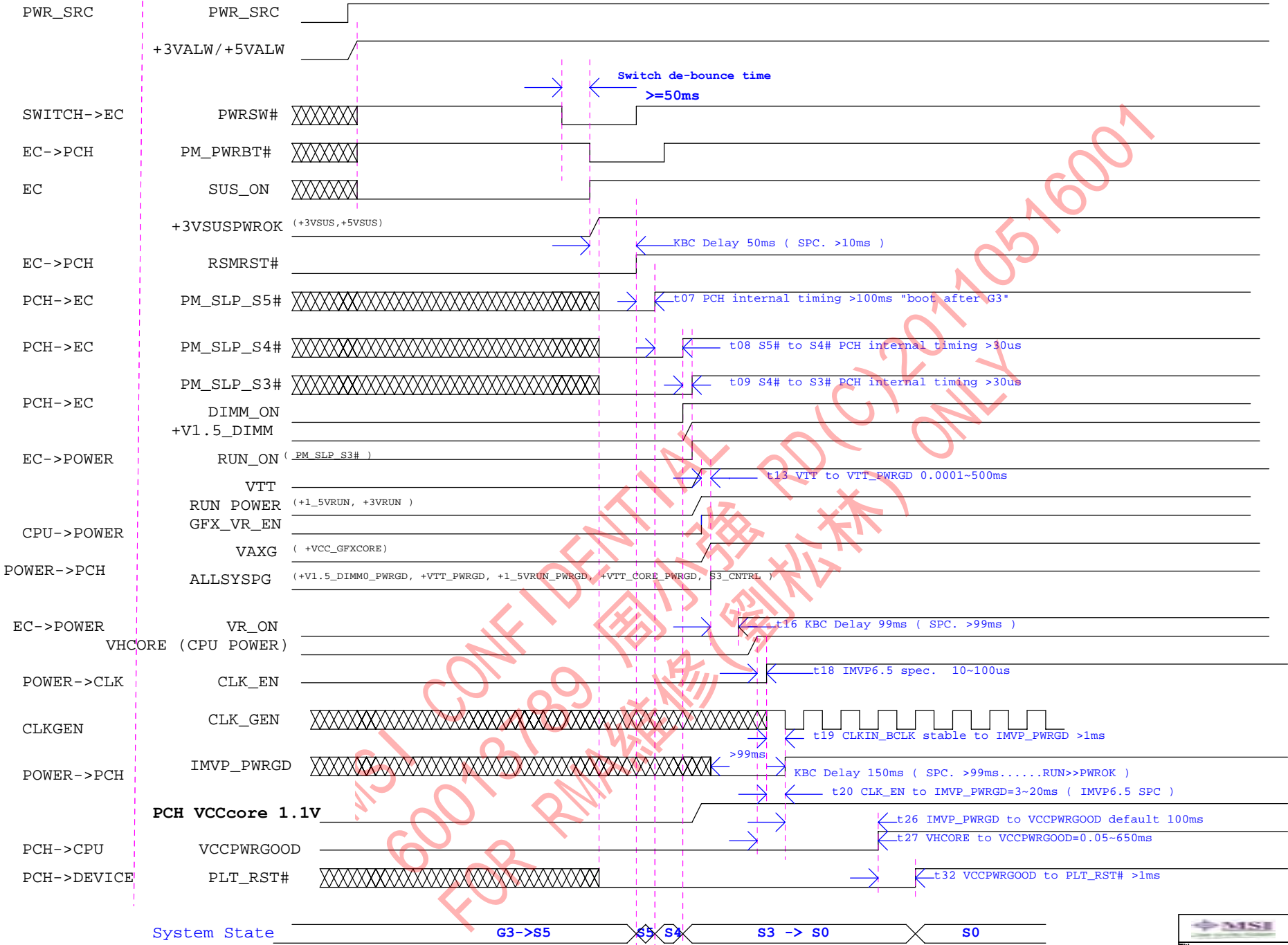


MICRO-STAR INT'L CO.,LTD.			
Title			
VTT Power,+1.8VRUN			
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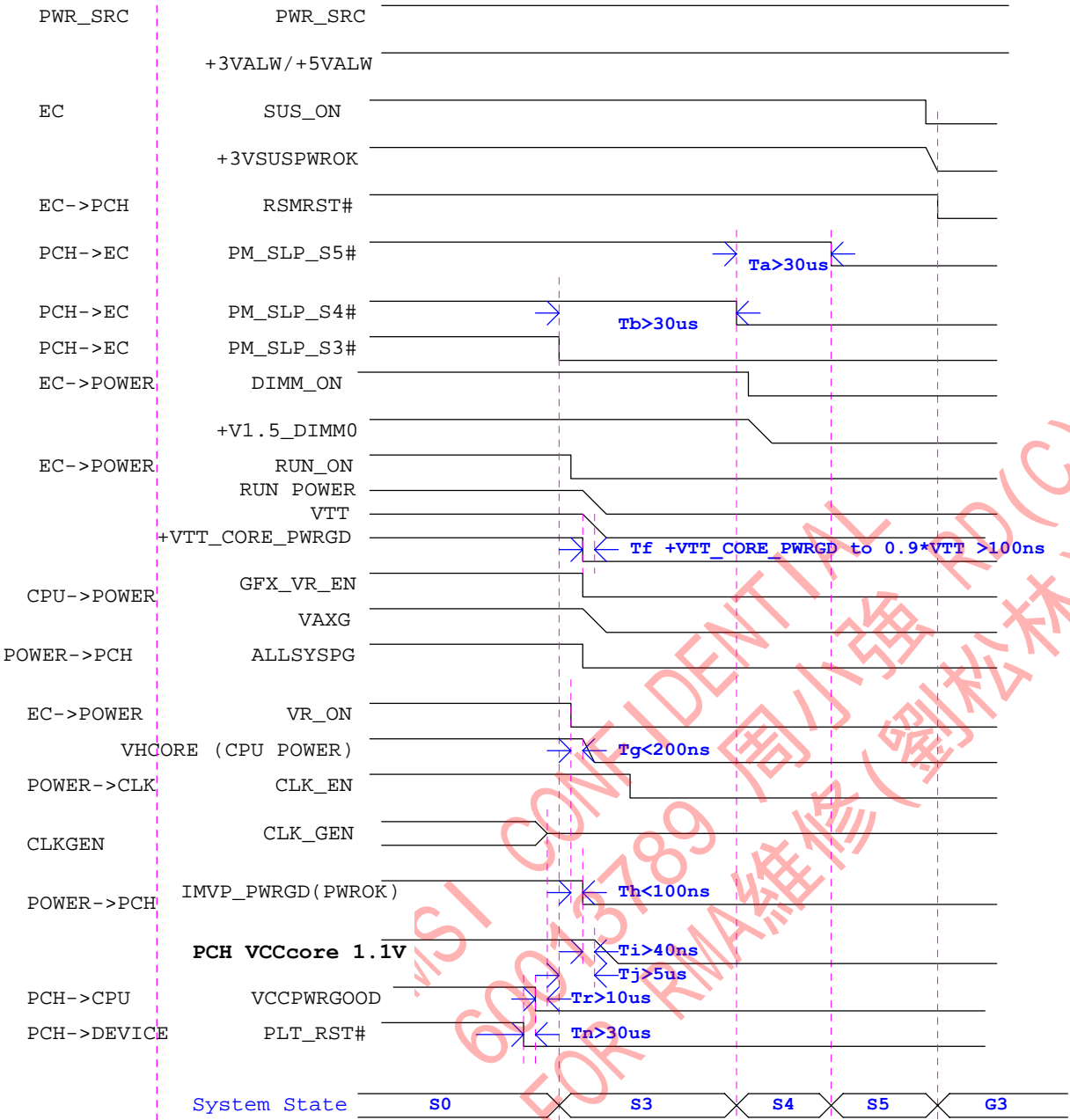




Calpella System Power on Sequence DC mode



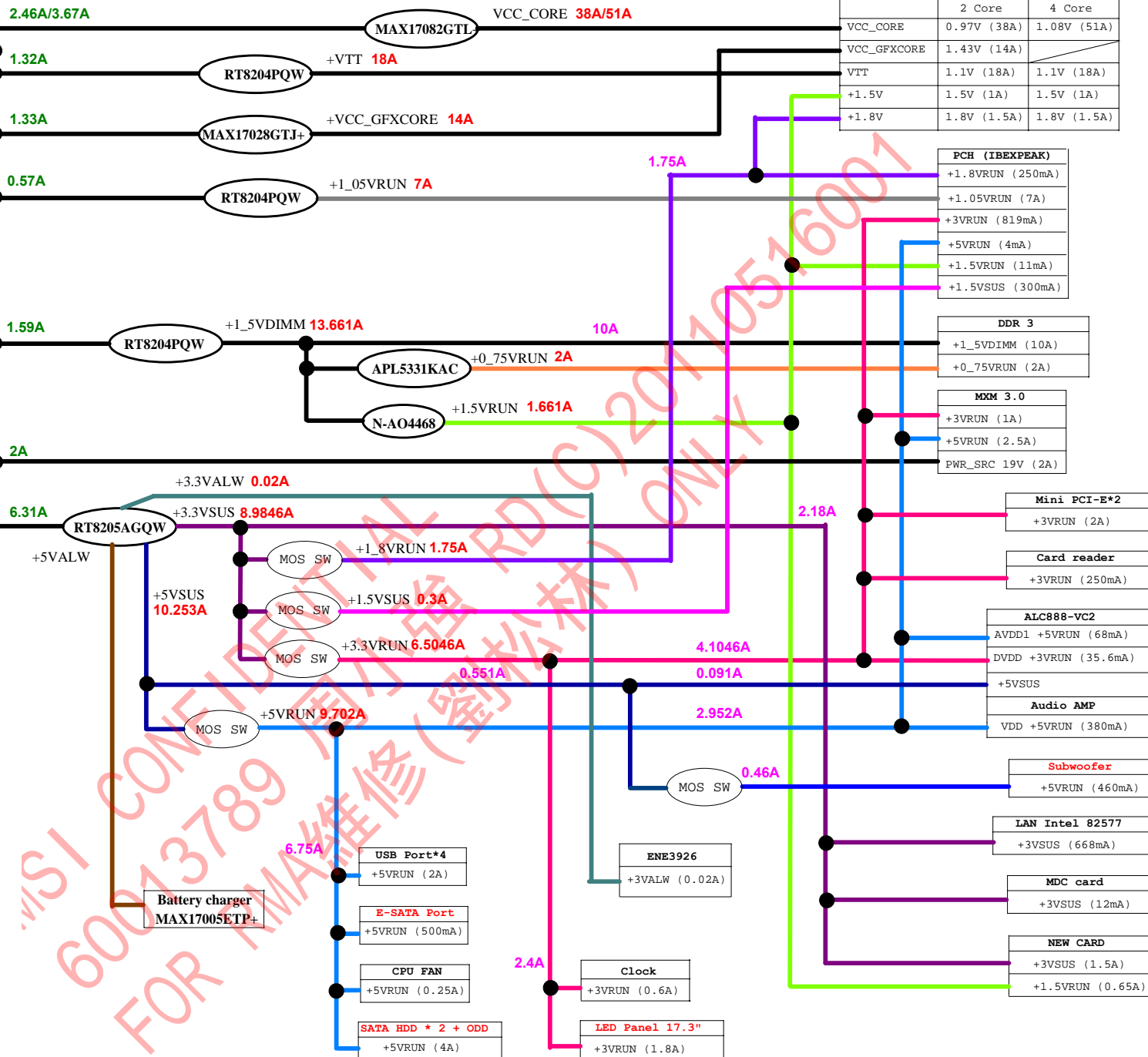
Power down Sequence DC mode S0 to G3



PWR_SRC

BAT : 3S2P = 9V
3S3P = 9V

VCC_CORE(2 Core) = 38A
VCC_CORE(4 Core) = 51A
+VTT(1.05V) = 18A
+VCC_GFXCORE = 14A
+1_05VRUN = 7A
+1_5VDIMM = 13.661A
+0_75VRUN = 2A
+1.5VRUN = 1.661A
+3.3VALW = 0.02A
+3.3VSUS = 8.9846A
+1_8VRUN = 1.75A
+1.5VSUS = 0.3A
+3.3VRUN = 6.5046A
+5VSUS = 10.253A
+5VRUN = 9.702A




2008/11/13 修改

Change Note :

0A-->0B

- 1.P19 stuff R113 & C85 for intel document about Braidwood
- 2.P23 add one PWM Pin for co-lay LED panel by EC
- 3.P25 Change CardReader to ENE
- 4.P26 Change "LED_HDD#" PU +5VRUN to +3VRUN
- 5.P26 Fan conn footprint change back to "53398_03"
- 6.P28 Add Wireless & Bluetooth combo(MS-3870)
- 7.P32 Change PR171 to 51.1K & PR172 to 1R0603
- 8.P33 Change PU2 from "UP6182AQAG" to "TPS51125" & PR18 to 30K
- 9.P34 Change PU9 from "UP6111AQDD" to "UP6128A" & PR156 to 3.48K & PR159 to 10.7K & PQ10 to "D03-0443033-V02"
- 10.P35 Change PU8 from "UP6111AQDD" to "UP6128A" & PR149 to 4.22K & remove C394
- 11.P36 Change PR95 to 1.82K & PR29 to 9.31K & PC90 to 47nf & PR99 to 931R & no stuff PC84 , PR94 , PEC4 , PEC5 , PEC6 , PEC8

		MICRO-STAR INT'L CO.,LTD.	
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NOTE			
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